Little Board™/486*e* Computer

P/N 5001561 Revision A

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REVISION HISTORY

Revision	Reason for Change	Date
1	Initial Release	2/00
A	Production Release	7/00

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Preface

Introduction

This manual is for designers of systems based on the Ampro Little Board™/486*e* single board system. This manual contains information that permits users to create an embedded system customized to specific requirements. Information includes:

- Hardware requirements
- Programming instructions
- Details for integrating it with other equipment

Technical Support

The Ampro Virtual Technician is available 24 hours a day at http://www.ampro.com, the Ampro Computers, Inc World Wide Web site. The Ampro Virtual Technician is a searchable database of Frequently Asked Questions. Look here first for your technical solutions.

The Ampro Engineering University is also available at the Web Site. Ampro Engineering University was created as a resource for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience. This page contains links to White Papers, Specifications, and additional technical information.

Ampro technical support is available from 8:00 AM to 5:00 PM, Pacific Standard Time, Monday through Friday. When calling for technical support, please have the product and it's technical manual available.

USA Technical Support Contact Information

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Chapter 1
Introduction

General Description

The Little Board™/486*e* CPU is an exceptionally high integration, high performance, 486DX-based PC/AT compatible system in the EBX form factor. This rugged and high quality single-board system contains all the component subsystems of a PC/AT motherboard plus the equivalent of six PC/AT expansion boards.

Key functions included on the Little Board/486*e* CPU are:

- CPU
- RAM
- Embedded-PC BIOS
- Keyboard and speaker interfaces
- Four buffered serial ports
- Multimode parallel port
- Floppy drive controller and local-bus IDE drive controllers
- Flat panel/CRT display interface
- Ethernet LAN interface

In addition, the Little Board/486*e* CPU includes a comprehensive set of system extensions and enhancements that are specifically designed for embedded systems. It is designed to meet the size, power consumption, temperature range, quality, and reliability demands of embedded applications.

Among the many embedded-PC enhancements that ensure fail-safe embedded system operation are a watchdog timer, a powerful NMI generator, and an onboard bootable “solid state disk” (SSD) capability. The unit requires a single +5 Volt power source and offers "green PC" power-saving modes under support of Advanced Power Management (APM) BIOS functions (APM Release 1.2-compliant).

Features

CPU/Motherboard

The Little Board/486*e* CPU implements a fully PC-compatible motherboard architecture, with an 80486 CPU running at 100 MHz or 133 MHz. The 486 CPU has an 8 Kbyte on-chip cache memory.

The board uses a standard 168-pin Dual In-line Memory Module (DIMM™) memory module, and supports up to 64M byte configurations. It has a full complement of standard PC/AT architectural features, including DMA channels, interrupt controllers, real-time clock, and timer counters.

VL-Bus Flat Panel/CRT Display Controller

A powerful and flexible local bus video display controller interfaces with both flat panels and CRTs, and offers full software compatibility with all popular PC video standards (VGA, Super VGA, and VESA). All standard resolutions up to 1280 x 1024 pixels and 16 million colors (True Color, in 640 x 480 VGA) are supported. Refer to Tables 3-1 and 3-2 for video specifications. 2M byte of video memory is standard. The display controller features:

- **High-speed VL-Bus Architecture.** The video controller provides an optimized 32-bit path between the CPU and video memory.
- **Graphical User Interface (GUI) Accelerator.** This feature can dramatically boost the performance of Windows®, Windows®9x, and many graphics-intensive applications.
- **Color Flat-Panel Support.** Up to 16M colors can be displayed on TFT LCD flat panels and up to 226,981 colors on STN LCD panels.
- **Display Centering and Stretching.** A variety of automatic display centering and stretching techniques can be employed when running lower resolution software on a higher resolution display.
- **Color Simulation/Reduction.** Color is automatically converted to gray-scale on most monochrome LCD panels, using a Frame Rate Modulation (FRM) and dithering techniques.
- **Standard Panel Support in the VIDEO BIOS.** The VIDEO BIOS supports a number of standard flat-panel displays, selectable from the system SETUP menu.

An optional external adapter board can provide an adjustable LCD bias power supply and power sequencing control.

Enhanced Embedded-PC BIOS

One of the most valuable features of the Little Board/486*e* CPU is its enhanced embedded-PC BIOS. Its extensive function set meets the unique requirements of embedded system applications. These enhancements include:

- Watchdog timer—monitors the boot process and provides a watchdog function call for applications
- Fast boot operation—normal or accelerated POST, selectable by SETUP options
- Configurable POST display—selects what displays at boot time
- Fail-safe boot support—intelligently retries boot devices until successful
- Battery-free boot support—saves system SETUP information in non-volatile EEPROM
- Serial console option—lets you use a serial device as a console
- Serial loader option—supports loading boot code from an external serial source
- EEPROM access function—512 bits of EEPROM storage available to user; useful for serialization, copy protection, and security
- OEM customization hooks—can execute custom code before system boot through ROM extensions; allows sophisticated system customization without BIOS modification

Serial Ports

Four PC-compatible RS-232C serial ports are standard. Serial Port features include:

- 16C550-type UARTs
- UARTs are equipped with 16-byte FIFO
- Support for 115K baud rates
- Onboard voltage converters provide the RS-232C voltage levels from the single 5 volt supply
- COM2 can be jumper configured to conform with RS-485

Enhanced Parallel Port

One PC parallel port is standard. It can be used for the following applications:

- Printer port
- Channel for access to parallel port interfaced peripherals
- Digital control (output) and sensing (input) lines
- EEP, ECP, SPP, and BPP Selectable

The parallel port can be:

- Set up as the primary or secondary parallel port using the BIOS SETUP function
- Disabled to free its PC resources for other peripherals

Floppy Interface

An onboard floppy disk interface provides access to standard floppy drives. The interface supports up to two 5.25 inch or 3.5 inch floppy drives in any combination.

IDE Interface

An onboard IDE interface provides high-speed hard disk and CD-ROM drive access. The interface supports up to two drives. The BIOS supports hard drives up to 8.4G bytes through Logical Block Addressing (LBA).

Compact Flash Disk

The Compact Flash interface allows you to substitute solid-state Flash memory for a conventional rotating-media drive. Any DOS-based application, including the operating system, utilities, drivers, and application programs, can easily be run from the Compact Flash device without modification

The Compact Flash disk is a solid-state disk system that emulates an IDE drive. It uses standard Compact Flash disk media, similar to a PCMCIA memory card, but smaller. Insert the Compact Flash disk media in the on-board Compact Flash socket, and use it in much the same way you would use a removable-media hard drive. The Compact Flash drive is architecturally equivalent to an IDE drive in your system. When installed, it becomes one of the two IDE drives supported by the primary EIDE disk controller. It can be configured as either an IDE master or slave drive.

Ethernet LAN Interface

The Ethernet LAN interface uses Carrier Sense, Multiple Access/Collision Detect (CSMA/CD) for node access and operates at a 10M-bits/second data rate. The Ethernet interface has the following features:

- Contains the logic necessary to send and receive data packets
- Controls CSMA/CD network access technology
- Meets IEEE 802.3 (ANSI 8802-3) Ethernet standards
- Supports the Ethernet twisted-pair standard (10BaseT)

Because Ethernet is preferred in many applications due to its high data rate and broad level of compatibility, Ampro supplies the Little Board/486*e* CPU with drivers and utilities to ensure compatibility with a wide range of popular operating systems and network operating systems. The Ethernet interface is based on the SMC9000-series single-chip Ethernet controller. DOS software drivers for ODI, NDIS, packet, and TCP/IP are supplied with the Little Board/486*e* Development Kit. OS support includes QNX, UNIX, Windows®9x, Windows NT™, Windows CE and DOS.

The Ethernet interface provides boot PROM capability. When implemented, the embedded system boots directly from the network, eliminating the need for a local floppy, hard drive, or SSD.

Byte-Wide Socket and Solid State Disk (SSD)

The byte-wide memory socket included with the Little Board/486*e* CPU allows you to install a bootable “solid state disk” (SSD) for installation of embedded application software. The SSD supports:

- EPROM
- FLASH EPROM
- Battery-backed SRAMs

Using Ampro’s SSD Support Software, any DOS-based application, including the operating system, utilities, drivers, and application programs, can be run from SSD without modification. SSD operation is also supported by a number of real-time operating systems.

The board’s 32-pin byte-wide socket accepts 32-pin byte-wide memory devices. It accommodates 128K bytes to 1M byte devices and supports:

- CMOS SRAM
- SRAM non-volatile modules
- EPROM
- FLASH EPROM

Modular PC/104 Expansion Bus

The Little Board/486*e* CPU provides a PC/104-compatible expansion bus for additional system functions. This bus is a compact version of the standard PC ISA bus and offers compact, self-stacking, modular expandability. The growing list of PC/104 modules available from Ampro and other PC/104 vendors includes such functions as:

- Communications interfaces
- Video frame grabbers
- Field bus interfaces
- Digital signal processors (DSPs)
- Data acquisition and control functions
- Many specialized interfaces and controllers

In addition, customized, application-specific logic boards can be stacked on top of the Little Board/486*e* CPU using the PC/104 expansion bus interface as a rugged and reliable interconnect. The PC/104 bus is an embedded system version of the signal set provided on a desktop PC's ISA bus.

Enhanced Reliability

Ampro specializes in producing highly reliable embedded system computers and peripherals capable of withstanding hostile, mission-critical environments without operator intervention. Ampro's system designs and a comprehensive testing program have evolved to ensure a reliable and stable system for use in these harsh and demanding applications.

ISO 9001 Manufacturing. Ampro is a certified ISO 9001 vendor.

Regulatory testing. Knowing that many embedded systems must qualify under EMC emissions susceptibility testing, Ampro designs boards with careful attention to EMI issues. Boards are tested in standard enclosures to ensure that they can pass such emissions tests. Tests include the following CE MARK European Union directives:

- EN55022 and EN55011 (for EMC)
- EN61000-4-2 (for ESD)
- EN61000-4-6 (for RF Susceptibility)
- EN61000-4-4 (For EFT)

Tests also include emissions testing at US voltages per FCC Part 15, Subpart J. The test levels are CISPR Class A / VCCI1, Light Industrial.

Wide-range temperature testing. Ampro Engineering qualifies all of its designs by extensive thermal and voltage margin testing.

3.3V CPU for greater high temperature tolerance. The board uses the latest low-voltage CPU technology to extend its temperature range and reduce cooling requirements.

Shock and Vibration Testing. Boards intended for use in harsh environments are designed for shock and vibration durability to MIL-STD 202F, Method 214A, Table 214I, Condition D at 5 minutes per axis for random vibration, and to MIL-STD 202F, Method 213B, Table 213-1, Condition A for resistance to mechanical shock.

HALT Testing

The Little Board/486*e* CPU was subjected to Highly Accelerated Life Testing (HALT) as a part of its Engineering Qualification. An independent firm using a standardized procedure performed testing.

HALT testing is used during the development of a product to identify its temperature and vibration Operating Limits and Destruct Limits. The stresses applied during this testing greatly exceed those expected during normal operation. The intent of the test is to subject the unit to progressively greater extremes of temperature, rapid thermal transitions, vibration (in six axes), and combined temperature stress and vibration until the unit fails, and then is ultimately destroyed.

The results of the test identify the elements of the design that are the weakest, and at what level of environmental stress the elements fail or are destroyed. This information is then used to improve the design of the product.

Software

The Little Board/486*e* CPU can use most commercial and public-domain software developed for the IBM PC and PC/AT. Software development tools such as editors, compilers, and debuggers can be used to develop application code. System requirements can be quickly tailored to your needs using these standard tools with the utilities and drivers supplied with each Little Board/486*e* CPU.

The board's SETUP function can be used for all system configuration tasks. SETUP can be invoked using the (CTRL-ALT-ESC) hot-key combination or by selecting the SETUP.COM utility program from the DOS command line. SETUP.COM is available on the Common Utilities diskette. Table 1–1 summarizes the configuration parameters you can modify using SETUP.

Table 1–1. Summary of SETUP Options

- Date and time in the battery-backed real-time clock
- Floppy drive quantity and type
- IDE Hard disk drive quantity and type
- Video controller
- Serial port enable/disable
- Parallel port address/disable
- Byte-wide socket
- Serial console option
- Video BIOS Shadow RAM enable
- DOS hard disk map
- Choice of default boot drive (hard disk or floppy)
- Enable/Disable hot-key access to SETUP
- Watchdog timer startup time-out
- Serial loader enable/disable/port selection
- POST speed options
- POST screen display and blanking options

SETUP information is stored in both the battery-backed CMOS RAM-portion of the real-time clock, and in a configuration EEPROM. A complete discussion of SETUP is provided in Chapter 2.

Little Board Development Platform

Whatever your Little Board application, there is always a need for an engineering development cycle. To help developers quickly assemble an embedded system, Ampro's Little Board Development Platform provides developers with tools to manage development and assembly for embedded system components such as:

- Power supplies
- Floppy disk drive
- Hard disk drive
- Speaker
- I/O connectors
- Two-slot PC backplanes

The Development Platform provides a *known good* environment for your development work. You can install the Little Board/486*e* CPU, MiniModules™ expansion products or conventional expansion boards, keyboards, monitors, and I/O devices to quickly create a platform for your hardware and software engineering needs. Often, Development Platforms are used in repair and support facilities as well, and on the production floor for system test. Contact your Ampro sales representative for additional information.

Chapter 2
Product Reference

Overview

This chapter contains the technical information required to install and configure the Little Board™/486*e* CPU. The information includes:

- Power Connector
- DRAM memory
- Serial Ports
- Bi-directional parallel port
- Floppy disk interface
- IDE hard disk interface (Compact Flash)
- Video Controller
- 32-pin byte-wide socket
- Ethernet local area network interface
- Utility connector (keyboard, PC speaker, reset button, external battery, PS/2 mouse)
- Watchdog timer
- Battery-backed clock
- PC/104-compatible expansion bus
- SETUP function

Interface Connector Summary

Refer to Figure 2–1 for the locations of the connectors (P1A/B, P2C/D, J2 – J7, J11 – J16) and configuration jumpers (W1 – W14). Table 2–1 summarizes the use of the I/O connectors and Table 2–2 summarizes use of the configuration jumpers. Each interface is described in its own section, showing connector pin outs, signal definitions, required mating connectors, and configuration jumper options.

Many of the connectors have a *key pin* removed. This allows you to block the corresponding cable connector socket to help prevent improper assembly and possible board damage. Table 2–1 indicates which pins are key pins, and Figure 2–1 shows their locations.

Table 2–1. Connector Usage Summary

Connector	Function	Size	Key Pin
P1A/B	PC/104 Expansion Bus	64-Pin	B10
P2C/D	PC/104 Expansion Bus	40-pin	C19
J2	Compact Flash Card	50-pin	
J3	Flat Panel Video	50-pin	35
J4	LCD Bias Supply Connector	12-pin	3, 10
J5	CRT Video	10-pin	None
J6	RS-485	2-pin	None
J7	Ethernet Twisted Pair	RJ45	None
J10	Power, +5V and +12V	4-pin Molex	None
J11	Serial 1 and Serial 2	20-pin	20
J12	IDE Hard Disk	40-pin	20
J13	Serial 3 and Serial 4	20-pin	20
J14	Floppy Interface	34-pin	6
J15	Parallel Port	26-pin	26
J16	Utility/Keyboard	16-pin	2

Connectors

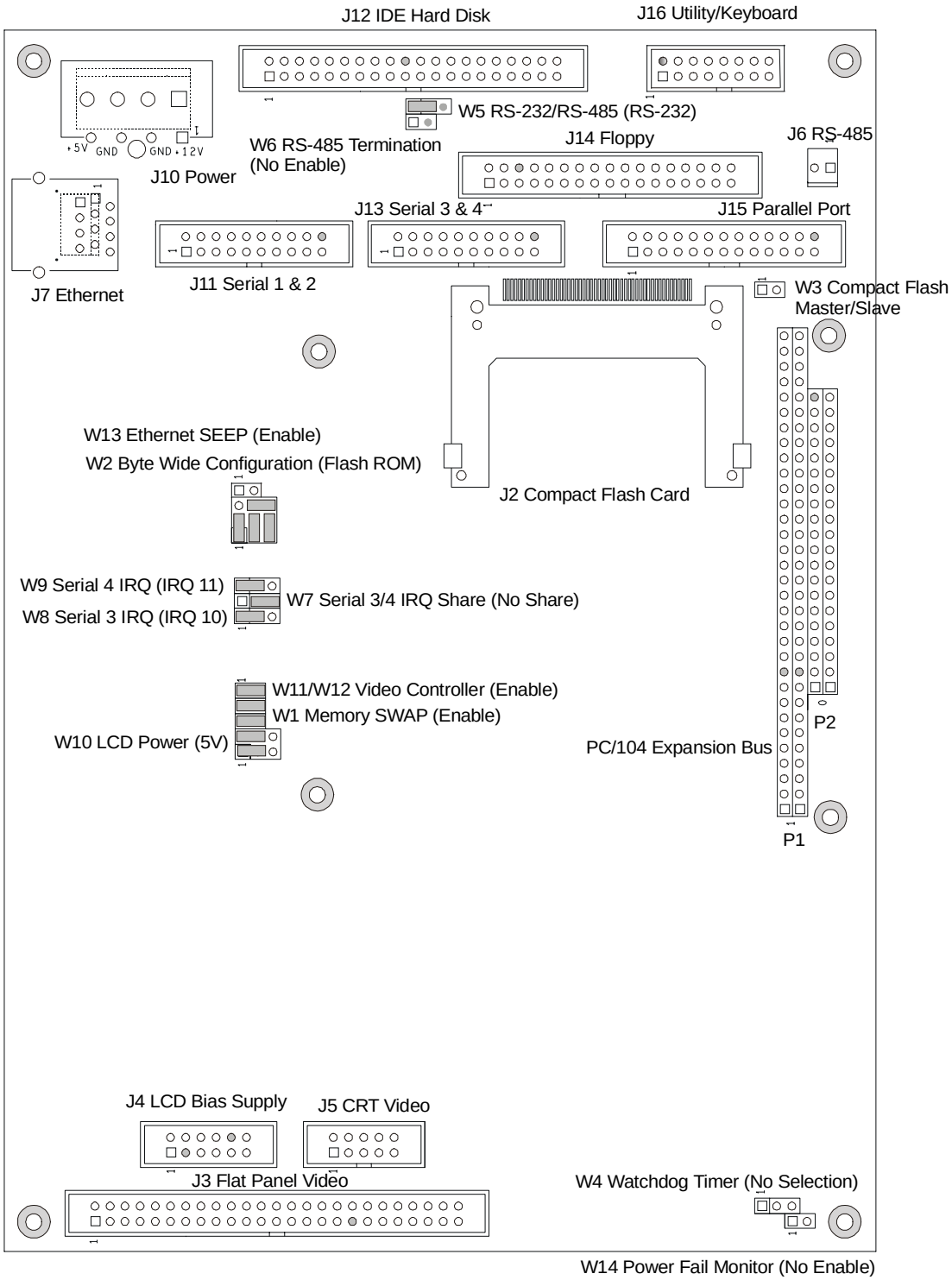
The I/O connectors are dual-row headers for use with insulation displacement connectors (IDC) and flat ribbon cable.

A number of the connectors have *key pins*. Install a blocking key in the corresponding connector socket on the mating ribbon cable to prevent misalignment.

You can design PC boards with female connectors in the same relative positions as the Little Board's connectors. This eliminates cables, meets packaging requirements, adds EMI filtering, or customizes the installation in other ways.

The PC/104-compatible expansion bus is located on connectors P1A/B and P2C/D. The system can be expanded using Ampro MiniModule expansion products or other PC/104-compliant expansion modules. These modules can be attached by stacking them directly on the P1 and P2 connectors or by using standard or custom expansion hardware; including solutions available from Ampro. Contact your Ampro sales representative for information about alternatives offered by Ampro.

If you plan to use the on-board video controller with a flat-panel LCD that requires a Vee voltage, you can install Ampro's optional LCD Bias Supply board on connector J4, as shown in Figure 2-1. This board can be jumpered to supply positive or negative Vee from ±15V to ±35V (adjustable).



Shaded connector pins indicate key pins. Default settings for jumpers are in parenthesis.)

Figure 2–1. Connector and Jumper Locations

Jumper Configuration Options

Ampro installs optional jumpers in default positions so that the Little Board/486*e* CPU requires no special jumpering for immediate operation. Jumper-pin arrays are designated W1, W2, and so forth. Jumper pins have a 2mm pitch. A square solder pad identifies pin 1 of each jumper array.

Table 2–2 provides a summary of jumper use. In the Default column, two numbers separated by a slash (for example, 1/2) means that pins 1 and 2 are shorted with a 2 mm jumper block.

Table 2–2. Configuration Jumper Summary

Jumper Group	Function	Default
W1	Memory SWAP	ON
W2	Byte-Wide S0 Configuration (default is Flash EPROM)	1 /2, 4/5, 7/8, 6/9
W3	Compact Flash Master/Slave Selector	OFF (Slave)
W4	Watchdog Timer Output Select (IOCHECK, Reset)	OFF (No Selection)
W5	Serial 2 RS-232/RS-485 Select	1/2 (RS-232)
W6	RS-485 Termination Enable	OFF (No Enable)
W7	Serial 3/4 IRQ Sharing	2/3 (Non-sharing)
W8	Serial 3 IRQ Selector	1/2 (IRQ 11)
W9	Serial 4 IRQ Selector	1/2 (IRQ 10)
W10	LCD Power Selector	1/3 and 2/4 (+5V)
W11/W12	Video Controller Enable	ON/ON (Enable)
W13	Ethernet SEEP Enable	OFF (Enable)
W14	Power Fail Monitor NMI Enable	OFF (No Enable)

System I/O Map

Table 2–3 lists the I/O port assignments of the Little Board/486*e* CPU. The I/O port functions and addresses are both hardware and software compatible for all standard PC applications.

The ROM BIOS typically provides all of the services needed to use the onboard and I/O port connected devices. If you need to directly program the standard functions, refer to a programming reference for the PC/AT.

Table 2–3. Little Board/486e I/O Map

I/O Address	Function
3F8h - 3FFh	Primary serial port
3F2h - 3F7h	Floppy disk controller ports 3F2: FDC Digital output register 3F4: FDC Main status register 3F5: FDC Data register 3F7: FDC Control register
3F0h - 3F1h	Ampro reserved
3E8h - 3EFh	Third serial port
3D0h - 3D7h, 3DA	Video controller
3C0h - 3CFh	Video controller
3B4, 3B5, 3BA	Video controller (MDA Emulation)
378h - 37Fh	Primary parallel printer port
320h - 32Fh	Ethernet interface (default)
2F8h - 2FFh	Secondary serial port
2F0h - 2F3h	Ampro reserved
2E8h - 2EFh	Fourth serial port
278h - 27Fh	Secondary parallel printer port
1F8h - 1FFh	Ampro reserved
1F0h - 1F7h	IDE hard disk interface
102	Video Controller (Global Enable)
0F0h - 0FFh	Reserved
0C0h - 0DFh	DMA controller 2 (8237 equivalent)
0A0h - 0A1h	Interrupt controller 2 (8359 equivalent)
092h	Fast A20 gate and CPU reset
080h - 08Fh	DMA page registers (74LS61 equivalent)
070h - 071h	Real-time clock and NMI mask
060h, 064h	Keyboard controller (8042 equivalent)
040h - 043h	Programmable timer (8254 equivalent)
020h - 021h	Interrupt controller 1 (8359 equivalent)
000h - 00Fh	DMA controller 1 (8237 equivalent)
E0E0h - E0EFh	Ethernet disable address (full 16-bit address)

Note

All I/O ports below 100h are reserved for internal system functions and should not be accessed.

DC Power

Power the module by connecting the DC power supply to the PC/104 expansion bus and connect the voltages to J10. Refer to Table 2–4 for power connections and Table 2–5 for mating connector information.

Table 2–4. J10 Power Connector

Pin	Connection
1	+12VDC ±5% input
2, 3	Ground return
4	+5VDC ±5% input

Table 2–5. J10 Mating Connectors

Connector Type	Mating Connector
Discrete Wire	AMP Housing 1-480424-0 AMP PIN 60619-1

Caution

Be sure the power plug is wired correctly before applying power to the board. See Figure 2–2.

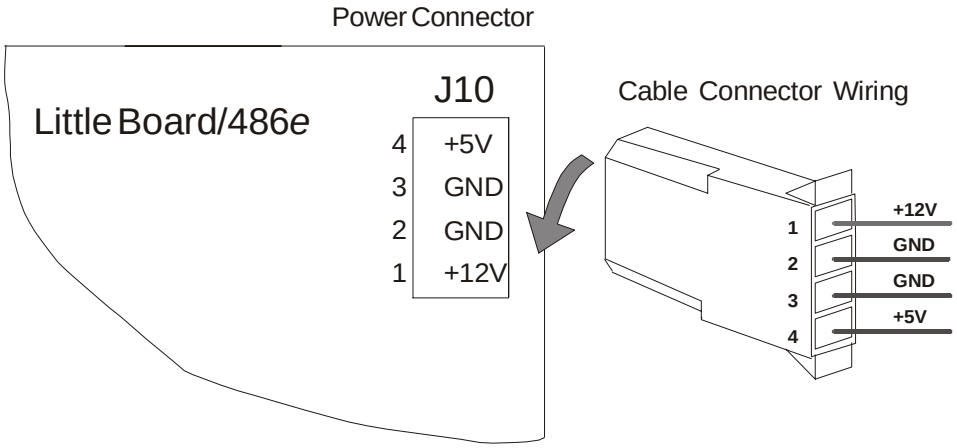


Figure 2–2. Power Connector Wiring

Power Requirements

The Little Board/486*e* CPU operates on +5VDC (±5%). The ±9V RS-232 voltages are generated on board. The exact power requirement of the Little Board/486*e* CPU system depends on several factors such as:

- Amount of installed DRAM
- Number of installed byte-wide memory devices
- Peripheral connections
- MiniModule products (if installed)
- Other expansion boards attached to the PC/104 bus

For example: AT keyboards draw power from the motherboard, and there can be some loading from the serial and parallel ports. Consult the specifications in Chapter 3 for the basic power requirements of your model.

If a switching power supply is used it must regulate properly with the system load. Some switching power supplies do not regulate properly unless they are loaded to some minimum value. If this is the case, consult the manufacturer for information regarding additional loading or use another supply or another type of power source such as a linear supply, or batteries.

Backup Battery

With only the real-time clock drawing current, the backup battery on the Little Board/486*e* should last 10 years. If it supplies only the clock, replace the battery every 10 years as a routine maintenance procedure.

Cooling Requirements

Adequate airflow should be provided to maintain an ambient temperature at or below 70°C within the case. For Extended Temperature Qualified products, the temperature must remain at or below 85°C. Little Board/486*e* CPU uses a 486DX/System Logic Chip rated at 3.3V to minimize power drain. In addition a heat sink is provided for the CPU. The majority of the current draw and heat generated come from the:

- 486 CPU
- DRAM
- video controller
- 486DX/System Logic Chip

Powerfail Monitor

The Little Board/486*e* CPU has a built-in powerfail circuit that generates a clean reset signal if power falls below 4.65V. It guarantees a minimum 140 mS reset signal, independent of how long the power falls below the 4.65V threshold.

To enable the powerfail circuitry, short W14 with a jumper.

Non-maskable interrupt (NMI): When the supply voltage falls below (approximately) 4.7 volts, the powerfail logic sends an NMI to the CPU. When the BIOS detects the NMI, it displays the message “Power Fail NMI” on the screen. You have two options at this point (made by keyboard selections). One is to mask the NMI and continue. The other is to reboot the system. This requires operator intervention. If you want an automatic response to the NMI, you can provide an NMI handler in your application, and patch the NMI interrupt vector address to point to your routine.

If you have configured the byte-wide socket S0 for battery backup, it will be write protected while power is below 4.7 volts. (Its chip select is held to a logic 1.) This is to prevent writing bad data to an SRAM in S0 when the voltage is low.

Hardware reset: If the supply voltage falls below (approximately) 4.40V, the powerfail logic initiates a hardware reset (like pressing the RESET button). A “clean” reset during a low voltage period prevents erratic operation or crashes. Reset is asserted for the duration of the low-voltage period plus 100 mS after the voltage returns to above 4.40V.

DRAM

There is no DRAM soldered on board. The Little Board/486*e* CPU will support up to 64M byte of system DRAM. A single vertical 168-pin DIMM socket supporting symmetrical EDO 3.3V modules is used.

When the system boots, the BIOS measures the amount of memory installed and configures the internal memory controller. No jumpering or manual configuration is required. The amount of memory found can be displayed by running SETUP. Saving SETUP automatically stores this figure in the Configuration Memory.

Note

If you change the amount of memory installed, you must run SETUP again to save the new value in the Configuration Memory.

Onboard memory is allocated as follows (standard for the PC architecture):

- The first 640K bytes of DRAM are assigned to the DOS region 00000h to 9FFFFh.
- DRAM in the top 384K bytes of the first 1M byte is not available for user programs. DRAM is mapped into the top 64K to shadow the ROM BIOS. DRAM can also be mapped into a portion of this region to shadow a video BIOS (a SETUP option).
- The remaining memory is mapped to extended memory starting at the 1M byte boundary.

System Memory Map

The Little Board/486*e* CPU address up to 64M bytes of memory. Table 2–6 shows how this memory is used.

The first megabyte stores the following data starting at memory address 00000h:

- DRAM
- Byte-wide socket
- ROM BIOS

Table 2–6. Little Board/486e Memory Map

Memory Address	Function
0100000h – 3FFFFFFh	Extended memory
00F0000h - 00FFFFFh	64K ROM BIOS
00D0000h - 00EFFFFh	Byte-wide socket S0, if enabled, otherwise, free
00CC000h – 00CFFFFh	Onboard BIOS Expansion Flash device for Ethernet boot PROM code
00C0000h - 00CBFFFh	Video BIOS for onboard flat panel video controller
00A0000h - 00BFFFFh	Normally contains video RAM, as follows: CGA Video: B8000-BFFFFh Monochrome: B0000-B7FFFh EGA and VGA video: A0000-AFFFFh
000000h - 09FFFFh	Onboard DRAM

Expanded Memory and Extended Memory

Extended memory is a contiguous linear block of memory above 1M byte. Some programs require that memory be available as *expanded* or *EMS memory*, which makes memory available as pages rather than as a contiguous block. The procedure for accessing expanded memory is defined in the EMS LIM 4.0 specification.

Expanded memory can be converted into EMS memory by using the EMS emulation utilities in DOS. Current versions of DOS provide EMS emulation utilities, such as EMM386, that conform to the LIM 4.0 specification. Refer to the DOS technical documentation for instructions for using the EMS emulation utility.

Serial Ports (J11, J13)

Four RS-232C serial ports are included on the Little Board/486*e* CPU. Serial port 2 provides an optional RS-485 serial interface. Both serial ports support software selectable standard baud rates up to 115.2K baud, 5-8 data bits, and 1, 1.5, or 2 stop bits. The IEEE RS232C specification limits the serial port to 19.2K baud on cables up to 50 feet in length. The serial ports are based on a 16550 UART-compatible controller. This is an advanced UART that has a 16-byte FIFO buffer to improve throughput.

RS-232C Serial Ports

The Little Board/486*e* CPU can use 5BC sometimes as an alternate computer. Microprocessor system provides four standard RS-232C serial ports at J11 and J13 for use with:

- Printers
- Modems
- Terminals
- Remote hosts
- Touch input devices
- Any RS-232C serial device

Many devices require handshaking in one or both directions. Consult the documentation for any device(s) used for information about handshaking, cabling, and other interface considerations. Information about serial port configuration using SETUP, is provided in this chapter.

RS-485 Serial Port

An RS-485 option is available for Serial Port 2 at J11. Use of the RS-485 option offers a low cost, easy-to-use communications and networking multidrop interface that is ideally suited to a wide variety of embedded applications requiring low-to-medium-speed data transfer between two or more systems.

I/O Addresses

Serial port addresses are fixed and can not be changed. Each serial port, however, can be independently disabled using the SETUP function, freeing its I/O addresses for use by other devices installed on the PC/104 expansion bus. Port addresses are shown in Table 2–7.

Table 2–7. Serial Port I/O Addresses and Interrupts

Port	I/O Address	Interrupt
Serial 1	3F8h - 3FFh	4
Serial 2	2F8h - 2FFh	3
Serial 3	3E8h – 3EFh	7 or 11
Serial 4	2E8h – 2EFh	5 or 10

Interrupt Assignments

Interrupt 4 (IRQ4) is assigned to Serial 1 and Interrupt 3 (IRQ3) to Serial 2. These assignments can be disabled, but they cannot be changed. Serial 3 and Serial 4 can share their interrupts, using a “wired-or” configuration, they can use independent IRQs, or they can be disabled and use no interrupt at all. Jumper options are provided to independently select the wired-or configuration or independent interrupts for Serial 3 and Serial 4. See Figure 2–3 through 2–5.

Figure 2–3. Shared Wired-Or Configuration

Figure 2–4. Serial 3 Interrupt Configuration (W8)

Figure 2–5. Serial 4 Interrupt Configuration (W9)

When a serial port is disabled, its IRQ is available to other peripherals installed on the PC/104 expansion bus.

ROM-BIOS Installation of the Serial Ports

The ROM BIOS normally supports Serial 1 as the DOS COM1 device, Serial 2 as the DOS COM2 device, and so on. If a serial port is disabled and there is no substitute serial port in the system, the ROM-BIOS assigns the COM designations as it finds the serial ports, starting from the primary serial port and searching to the last one. For example, if Serial 1 is disabled, the ROM-BIOS assigns COM1 to Serial 2 (unless another Serial 1 is discovered). The ROM BIOS scans I/O addresses for serial ports in the following order: 3F8h, 2F8h, 3E8h, and 2E8h.

Serial Port Connectors (J11, J13)

Serial 1 and Serial 2 appears on connector J11. Serial 3 and Serial 4 appear on connector J13. Both connectors are wired the same, J11 for serial 1 and 2, and J13 for serial 3 and 4. Table 2–8 details the connector pinout and signal definitions for both ports. The table also identifies the pin numbers where each signal must be wired for compatibility with standard DB25 and DB9 connectors. A flat ribbon cable connects the header to a standard DB9 connector.

Note

PC serial ports are typically equipped with male DB9 connectors.

Table 2–8. Serial Port Connectors (J11, J13)

Ports	Pin	Signal Name	Function	In/Out	DB25 Pin	DB9 Pin
Serial 1 (J11) or Serial 3 (J13)	1	DCD	Data Carrier Detect	IN	8	1
	2	DSR	Data Set Ready	IN	6	6
	3	RXD	Receive Data	IN	3	2
	4	RTS	Request To Send	OUT	4	7
	5	TXD	Transmit Data	OUT	2	3
	6	CTS	Clear to Send	IN	5	8
	7	DTR	Data Terminal Ready	OUT	20	4
	8	RI	Ring Indicator	IN	22	9
	9	GND	Signal Ground	-	7	5
	10	N/A	No Connection	-	-	-
Serial 2 (J11) or Serial 4 (J13)	11	DCD*	Data Carrier Detect*	IN	8	1
	12	DSR	Data Set Ready	IN	6	6
	13	RXD	Receive Data	IN	3	2
	14	RTS	Request To Send	OUT	4	7
	15	TXD	Transmit Data	OUT	2	3
	16	CTS	Clear to Send	IN	5	8
	17	DTR	Data Terminal Ready	OUT	20	4
	18	RI	Ring Indicator	IN	22	9
	19	GND	Signal Ground	-	7	5
	20	N/A	Key Pin	-	-	-

Table 2–9 shows the manufacturer's part number for ribbon cable mating connectors to J11 and J13.

Table 2–9. J11 and J13 Mating Connector

Connector Type	Mating Connector
Ribbon	3M 3421-7600
Discrete Wire	MOLEX Housing 22-55-2202 Pin 16-02-0103

Configuring Serial 2 for RS-485 (J6, W5, W6)

Serial 2 provides circuitry for both an RS-232C and RS-485 interface. The port can be configured to support either interface using jumpers. The RS-232C interface appears on J11. The RS-485 interface appears on the two-pin connector, J6. Table 2–10 shows the pinout for J6. Table 2–11 shows the manufacturer's part number for mating connectors to J6.

Table 2–10. RS-485 Serial Port 2 Connector (J6)

Pin	Signal Name
1	+I/O
2	-I/O

Table 2–11. J6 Mating Connector

Connector Type	Mating Connector
Discrete Wire (Locking Connector)	MOLEX Housing 22-01-2027 Pin 08-55-0102

Figure 2–6 shows how to set W5 to select the output interface for Serial 2.

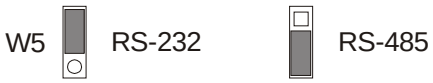


Figure 2–6. Serial 2 Interface Selection

Note

The RS-485 and RS-232C interfaces share the same circuitry. If you configure Serial 2 for RS-485, do not connect a serial device to J11. Similarly, if you configure Serial 2 for RS-232C, do not connect anything to J6.

The RS-485 interface specification requires that both ends of the twisted-pair cable be terminated with 100-ohm resistors. You can terminate the RS-485 interface on J6 with a resistor provided on the Little Board/486*e* CPU. To terminate the line, install a jumper on W6, see Table 2–12.

Table 2–12. RS-485 Termination using W6

W4	Result
On	Connects a 100 ohm termination resistor across J10
Off	No termination

RS-485 Twisted-Pair Cabling Using RJ11 Connectors

Connector J6 is used for an RS-485 twisted-pair connection. In RS-485 multidrop installations, standard RJ11 modular telephone connector jacks are often used to attach standard twisted-pair cables between systems.

RJ11 modular connectors have 6 available contact positions, but only 4 are populated. The 4 center conductors are wired so that the two outside and the two inside conductors are connected together. This eliminates any confusion about pin numbering conventions, as a reversal of connections has no effect. In addition, the lines were chosen to minimize the possibility of circuit damage should the unit be accidentally plugged into a standard telephone outlet. It sets the phone line to its *offhook* state to prevent the phone from ringing.

The recommended wiring for a J6-to-RJ11 cable is shown in Table 2–13.

Table 2–13. J6/RJ11 Cable Wiring

J6 Pin	RJ11 Pin	Signal	Standard Wire Color
	1	N/C	
2	2	- I/O Signal	Black
1	3	+ I/O Signal	Red
1	4	+ I/O Signal	Green
2	5	- I/O Signal	Yellow
	6	N/C	

When connecting the RS-485 port into a multidrop network, the devices at both ends of the network should be terminated with a 100 ohm resistor. Installing a jumper on W6 connects a termination resistor across the RS-485 line on the Little Board/486*e* CPU.

Using the RS-485 Interface

The RS-485 interface allows half-duplex operation using a 5 VDC differential interface. This interface provides greater immunity against noise and interference than single-wire interfaces and can drive cable lengths up to 4000 feet reliably at 57.6K bps. All communication, both transmission and reception, occurs through a single pair of wires. There are no handshaking lines.

RS-485 supports multidrop operation, where more than two devices can be connected to the same RS-485 balanced line. To prevent signal contention, only one transmitter is enabled at a time. The Little Board/486*e* RS-485 transmitter is controlled by Serial 2's RTS signal. At power up, RTS is in its inactive state, ready to receive. When it is time to transmit, the RTS signal is made active, enabling the transmitter. It is the responsibility of the user's software to prevent two transmitters from being enabled at the same time.

Figure 2–7 illustrates the Little Board/486*e* RS-485 interface wiring.

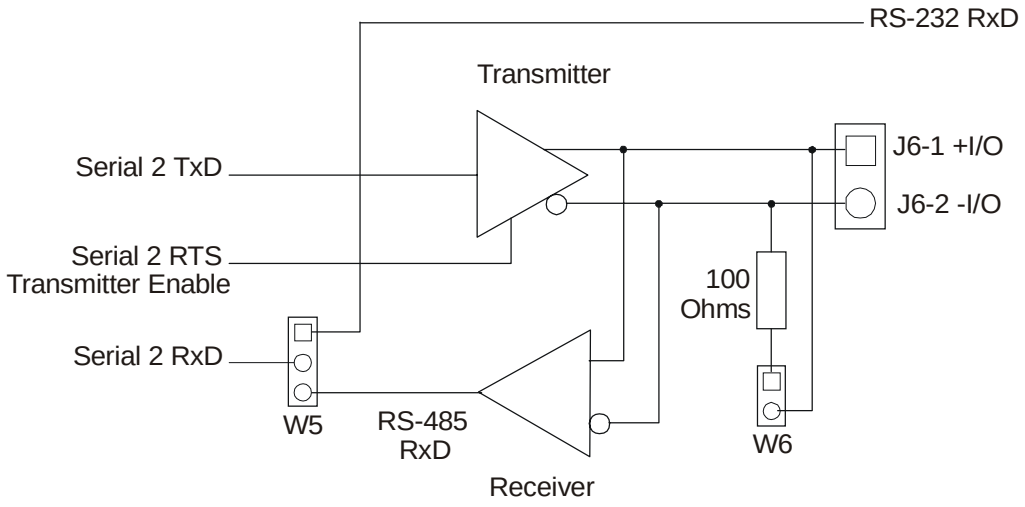


Figure 2–7. RS-485 Interface Wiring

Interconnection Scheme Examples

The following interconnection scheme examples take advantage of the RS-485 serial connection:

One-way Broadcast

A single device uses an RS-485 signal pair to transmit data to many receiving devices. When the RTS signal is turned on (True, High, and Active) and left on, the broadcast transmitter is enabled. If the device is to be a receiver, RTS must be turned off and left off.

Simple Bi-Directional Communication

Two devices using a single RS-485 bi-directional pair for half-duplex provide two-way transmission of data. The transceiver is placed in the send or receive mode under control of the network software using either a simple alternation scheme or by messages contained within data packets.

Multidrop Network

More than two devices share an RS-485 signal pair, for both transmission and reception of data. Only one device is permitted to talk at any one time. As with simple bi-directional communication, the board's RS-485 transceiver is placed in receive mode unless it is the one permitted to transmit. One popular way of managing who is the transmitter is by a "token" passing scheme. Each node is assigned an ID number. Whoever transmits also sends the ID of the next node allowed to transmit. If a node does not need to transmit, it just immediately sends the "token" to its next node. This simple scheme is easy to implement and trouble free. Time-outs can be implemented in software to prevent a lockup should a node fail to pass the token properly.

Serial Console

Ampro's unique ROM BIOS support for a serial console consisting of a keyboard and display replaces conventional video controllers, monitors, and keyboards. To use the serial console features, connect the serial console device(s) to Serial 1 or Serial 2. Use SETUP to configure the Little Board/486*e* CPU to use its serial console support feature. The configuration memory stores serial console configuration parameters.

Caution

Be careful when changing the console configuration using SETUP. If you specify "None" for console input and output, there is no console access to the system. (You can recover from this state by removing the serial console plug from the primary serial port connector and shorting pins J11-7/8.)

SETUP provides separate configurations for serial console input and outputs (I/Os) so that either input or output or both input and output are possible from any serial port and it's attached serial device.

To use an ASCII terminal as the console device for your system, set both the I/O parameters to Serial Port 1 (or 2), and set the serial baud rate, data length, and stop bits to match the setting of your terminal. For proper display of SETUP and POST messages from the BIOS, you must use an IEEE-compatible terminal that implements the standard ASCII cursor commands. The required commands and their hexadecimal codes are listed in Table 2–14.

Table 2–14. Required Commands

Hex	Command
08	Backspace
0A	Line Feed
0B	Vertical Tab
0C	Non-destructive Space
0D	Carriage Return

Note

Some programs that emulate an ASCII terminal do not properly support the basic ASCII command functions shown in Table 2–14. Ampro provides a suitable PC terminal emulator program, TVTERM, on the Common Utilities diskette.

The keyboard and screen of the terminal become the system console after system boots. Programs used this way must use ROM BIOS video functions rather than direct screen addressing for their display I/O. Keyboard data from both the external serial device and the standard AT keyboard can be entered.

Note

DOS programs that write directly to video RAM do not display properly on a serial console device.

COM Port Table

When the system boots DOS initializes the serial ports to 9600 baud (typical). To preserve the selected console port parameters stored in SETUP, the ROM BIOS can be instructed to delete the selected console port from the internal COM port table, normally used by DOS to locate the serial ports. With the port deleted from the COM port table, DOS cannot change its parameters. If you use a serial console, be sure to select the option that deletes the console port from the COM port table.

Serial Handshake

The serial console device data format and the Little Board/486*e* CPU serial port data format must match for the devices to properly communicate. In addition, the hardware handshake behavior must be compatible. Normally, a serial port's Data Set Ready (DSR) and Clear To Send (CTS) input handshake signals must be true (active) for the ROM BIOS to send data out. On the Little Board/486*e* CPU, the hardware handshake can be enabled or disabled with SETUP. When hardware handshaking is enabled, be sure to connect the DSR and CTS signals to appropriate handshake signals on the external serial device's interface connector. As an alternative, loop the Little Board/486*e* CPU's serial output handshake signals to its input signals as follows:

- DTR (out) to DSR (in)
- RTS (out) to CTS (in)

Serial Booting and Serial Programming

Serial console functionality has been expanded to incorporate two additional features useful in embedded applications.

- The *serial boot* facility enables the Little Board/486*e* CPU to boot from code downloaded through a serial port in a manner similar to booting from a local hard disk or from a network.
- The *serial programming* facility permits updating FLASH memory devices installed in the byte-wide socket over the serial port.

Refer to the Ampro Common Utilities manual for descriptions of Ampro's SERLOAD and SERPROG utilities used to support serial booting and serial programming.

Using a Serial Modem

Any RS-232C port can be used as a modem interface. Serial port initialization is not an issue since most PC communications programs control the serial port hardware directly. If the program does not handle serial port hardware in this manner, use the DOS MODE command to initialize the port.

Connect the appropriate I/O handshake signals required by the communications software when installing a modem. Standard PC-compatible, serial modem cables that connect all of the proper signals correctly are commonly available.

Many powerful communications programs are available to control modem communications. Some of these programs offer powerful *script* languages that allow you to generate complex automatically functioning applications with little effort.

Bi-Directional Parallel Port

The Little Board/486*e* CPU incorporates a standard PC bi-directional parallel port at connector J15. This port supports two modes of operation:

- Standard PC/AT printer port (output only)
- PS/2 compatible bi-directional parallel port (SPP)

Information about parallel port configuration using SETUP, is provided in this chapter. The low-level software interface to the parallel port consists of three addressable registers. The address map of these registers is shown in Table 2–15.

Table 2–15. Parallel Port Register Map

Register Name	Address	
	Primary	Secondary
Data Port	378h	278h
Status Port	379h	279h
Control Port	37Ah	27Ah

I/O Addresses

Four I/O ports control the parallel port functions. Enabling the base I/O address permits configuration of the primary parallel port (typically LPT1), the secondary parallel port (typically LPT2), or you can disable the port to free its hardware resources for other peripherals you install on the PC/104 bus. Table 2–16 lists the resources used by the parallel port.

Table 2–16. Parallel Port Configuration

Selection	I/O Address	Interrupts
Primary	378h - 37Fh	IRQ 7
Secondary	278h - 27Fh	IRQ5
Disable	None	N/A

ROM-BIOS Installation of Parallel Ports

LPT1 is normally assigned to the primary parallel port by the BIOS, LPT2 to the secondary parallel port if present, and so on. However, the BIOS scans the standard addresses for parallel ports and assigns LPT designations in the order it finds them. Thus, a secondary parallel port (at address 278h) can be assigned LPT1 if there is no primary port.

Note

The scan order is 3BCh, 378h, 278h.

Standard and General Purpose I/O Operation

The parallel port can be used as a standard output-only printer port or as a general-purpose digital I/O data port (Table 2–17). The bi-directional mode can be very valuable in custom applications; it might be used to control one of the following:

- Parallel-connected external peripherals
- An LCD display
- Scan keyboards
- Sense switches
- Interface with optically isolated I/O modules

All data and interface control signals are TTL-compatible.

Table 2–17. Parallel Port Use

Signal Type	Number of Lines	Function	Output Drive
Data	8 lines	Write Only	24 mA @ .5V 12 mA @ 2.4V
Control	4 lines	Read/Write	12 mA @.5V 4.7K PU
Status	5 lines	Read Only	--

The Bi-directional control register can be directly accessed without using the BIOS. The base address is 37Ah when the port is configured as the primary parallel port, and 27Ah when the port is configured as the secondary parallel port. Changing bit 5 can dynamically change the port between input and output modes. A “1” in bit five sets the port to input; a “0” sets it to output. The following example code dynamically changes the primary parallel port’s direction. The code assumes that the port is in Extended Mode.

```
;-------------------------------------------------------
; Code to change the parallel port direction to input
;-------------------------------------------------------
MOV   DX,37Ah
IN    AL,DX
OR    AL,20h           ;set bit 5
OUT   DX,AL
;
;-------------------------------------------------------
; Code to change the parallel port direction to output
;-------------------------------------------------------
MOV   DX,37Ah
IN    AL,DX
AND   AL,0DFh          ;clear bit 5
OUT   DX,AL
```

Parallel Port Interrupt

The parallel port can be configured to generate an interrupt request upon a variety of conditions. In most applications, the interrupt is not used. The standard parallel port interrupts are IRQ7 for the primary port and IRQ5 for the secondary port. The IRQ channel assignments are standard and cannot be changed. A bit in the parallel port's command registers enables or disables the port's connection to its interrupt line.

Parallel Port Interrupt Enable

Bit 4 in the control register (see Table 2–18) enables the parallel port interrupt. If this bit is high, then a rising edge on the -ACK (IRQ) line produces an interrupt on the interrupt IRQ7 (or IRQ5 if configured as the secondary port). .

Table 2–18. Parallel Port Register Bits

Register	Bit	Signal Name or Function	In/Out	Active High/Low	J15 Pin	DB25F Pin
DATA (378h)	0	Data 0	I/O	High	3	2
	1	Data 1	I/O	High	5	3
	2	Data 2	I/O	High	7	4
	3	Data 3	I/O	High	9	5
	4	Data 4	I/O	High	11	6
	5	Data 5	I/O	High	13	7
	6	Data 6	I/O	High	15	8
	7	Data 7	I/O	High	17	9
STATUS (379h)	0	0	In	---	---	---
	1	0	---	---	---	---
	2	0	---	---	---	---
	3	-ERROR	In	Low	4	15
	4	SLCT	In	High	25	13
	5	PE	In	High	23	12
	6	-ACK (IRQ)	In	Low	19	10
	7	BUSY	In	High	21	11
CONTROL (37Ah)	0	-STROBE	Out	Low	1	1
	1	-AUTOFD	Out	Low	2	14
	2	-INIT	Out	High	6	16
	3	SLC	Out	High	8	17
	4	IRQE	---	High	---	---
	5	PCD	---	High	---	---
	6	1	---	---	---	---
	7	1	---	---	---	---

Parallel Port Connector (J15)

Connection to the parallel port is through connector J15. Table 2–19 details the J15 pinout and signal definitions. Use a flat ribbon cable between J15 and a female DB25 connector. The table describes the connections from the header pins to the DB25 connector. Table 2–20 gives manufacturer's part numbers for mating connectors for J15.

Table 2–19. Parallel Port Connector

J15 Pin	Signal Name	Function	In/Out	DB25 Pin
1	-STROBE	Output data strobe	OUT	1
3	Data 0	LSB of printer data	I/O	2
5	Data 1		I/O	3
7	Data 2		I/O	4
9	Data 3		I/O	5
11	Data 4		I/O	6
13	Data 5		I/O	7
15	Data 6		I/O	8
17	Data 7	MSB of printer data	I/O	9
19	-ACK	Character accepted	IN	10
21	BUSY	Cannot receive data	IN	11
23	PAPER OUT	Out of paper	IN	12
25	SEL OUT	Printer selected	IN	13
2	-AUTOFD	Autofeed	OUT	14
4	ERROR	Printer error	IN	15
6	-INIT	Initialize printer	OUT	16
8	SEL IN	Selects printer	OUT	17
26	N/A	Key pin		
10,12,14, 16,18,20, 22,24	GROUND	Signal ground	N/A	18-25

Table 2–20. J15 Mating Connector

Connector Type	Mating Connector
Ribbon	3M 3399-7600
Discrete Wire	MOLEX Housing 22-55-2262 Pin 16-02-0103

Note

For maximum reliability, keep the cable between the board and the device it drives to 10 feet or less in length.

Register Bit Definitions

Table 2–21 defines the register bits shown in the **Signal Name** or **Function** column of Table 2–19.

Table 2–21. Standard and PS/2 Mode Register Bit Definitions

Signal Name	Full Name	Description
-ERR	Error	Reflects the status of the -ERROR input. 0 means an error has occurred.
SLCT	Printer selected status	Reflects the status of the SLCT input. 1 means a printer is on-line.
PE	Paper end	Reflects the status of the PE input. 1 indicates paper end.
-ACK	Acknowledge	Reflects the status of the ACK input. 0 indicates a printer received a character.
-BUSY	Busy	Reflects the complement of the BUSY input. 0 indicates a printer is busy.
STROBE	Strobe	This bit is inverted and output to the -STROBE pin.
AUTOFD	Auto feed	This bit is inverted and output to the -AUTOFD pin.
-INIT	Initiate output	This bit is output to the -INIT pin.
SLC	Printer select input	This bit is inverted and output to the pin. It selects a printer.
IRQE	Interrupt request enable	When set to 1, interrupts are enabled. An interrupt is generated by the positive-going -ACK input.
PCD	Parallel control direction	When set to 1, port is in input mode. In printer mode, the printer is always in output mode regardless of the state of this bit.
PD0-PD7	Parallel Data Bits	

Floppy Disk Interface

The onboard floppy disk controller and ROM BIOS support one or two floppy disk drives in any of the standard DOS formats shown in Table 2–22.

Table 2–22. Supported Floppy Formats

Capacity	Drive Size	Tracks	Data Rate
360K	5-1/4 inch	40	250 kHz
1.2M	5-1/4 inch	80	500 kHz
720K	3-1/2 inch	80	250 kHz
1.44M	3-1/2 inch	80	500 kHz

Floppy Drive Considerations

Nearly any type of soft-sectored, single or double-sided, 40 or 80 track, 5-1/4 inch or 3-1/2 inch floppy disk drive is usable with this interface. Using higher quality drives improves system reliability. Some considerations about the selection, configuration, and connection of floppy drives to the Little Board/486*e* CPU include:

- **Drive Interface**—The drives must be compatible with the board's floppy disk connector signal interface, as described below. Ampro recommends any standard PC-or AT-compatible 5-1/4 inch or 3-1/2 inch floppy drive.
- **Drive Quality**—High quality DC servo direct drive motor floppy disk drives must be used.
- **Drive Select Jumpering**—Jumper both drives for the second drive select (standard on PC drives).
- **Floppy Cable**—For systems with two drives, a floppy cable with conductors 10-16 twisted between the two drives must be used. This is standard practice for PC-compatible systems.
- The Little Board/486*e* CPU has a 2mm floppy port connector. The development kit contains an adapter board and a 2-mm cable that can connect the floppy drive to the Little Board/486*e* CPU. The adapter board has an additional connector that can connect a second floppy drive.
- **Drive Termination**—Resistive terminations should be installed only on the drive connected to the last interface cable connector (farthest from the board). Near-end cable termination is provided on the Little Board/486*e* CPU.
- **Head Load Jumpering**—When using drives with a Head Load option, the drive must be jumpered for head load with motor on rather than head load with drive select. This is the default for PC-compatible drives.
- **Drive Mounting**—If a floppy drive is mounted very close to the Little Board or another source of electromagnetic interference (EMI), a thin metal shield may need to be placed between the disk drive and the device to reduce the possibility of EMI.

Floppy Interface Configuration

The floppy interface is configured using SETUP to set the number and type of floppy drives connected to the system. Refer to the SETUP section later in this chapter for details.

If the floppy interface is not used, disable it in SETUP. This frees its I/O addresses (3F0h - 3F7h), DMA2, and IRQ6 for use by other peripherals installed on the PC/104 bus.

Floppy Interface Connector (J14)

Table 2–23 shows the pinout and signal definitions of the floppy disk interface connector, J14. The pinout of J14 meets the AT standard for floppy drive cables. Table 2–24 shows the manufacturer's part numbers for mating connectors.

Table 2–23. Floppy Disk Interface Connector (J14)

Pin	Signal Name	Function	In/Out
2	RPM/-RWC	Speed/Precomp	OUT
4	N/A	(Not used)	N/A
6	N/A	Key pin	N/A
8	-IDX	Index Pulse	IN
10	-MO1	Motor On 1	OUT
12	-DS2	Drive Select 2	OUT
14	-DS1	Drive Select 1	OUT
16	-MO2	Motor On 2	OUT
18	-DIRC	Direction Select	OUT
20	-STEP	Step	OUT
22	-WD	Write Data	OUT
24	-WE	Write Enable	OUT
26	-TRKO	Track 0	IN
28	-WP	Write Protect	IN
30	-RDD	Read Data	IN
32	-HS	Head Select	OUT
34	-DCHG	Disk Change	IN
1-33	(all odd)	Signal grounds	N/A

Table 2–24. J14 Mating Connector

Connector Type	Mating Connector
Ribbon	3M 3414-7600
Discrete Wire	MOLEX Housing 22-55-2342 PIN 16-02-0103

IDE Hard Disk Interface

The Little Board/486*e* CPU provides an interface for one or two Integrated Device Electronics (IDE) hard disk drives. IDE drives, the most popular and cost-effective type of hard drive currently available, have an internal hard disk controller. There are also many CD-ROM drives designed to use the IDE interface. If you attach a CD-ROM drive to the IDE port, you need a driver (supplied by the CD-ROM drive manufacturer) to access the device.

IDE Connector (J12)

The IDE interface appears at connector J12 a 40-pin, dual-row connector. Table 2–25 shows the interface signals and pin outs for the IDE interface connector. Table 2–26 shows manufacturer's part numbers for mating connectors to J12.

Note

For maximum reliability, keep IDE drive cables less than 18 inches long.

Table 2–25. IDE Drive Interface Connector (J12)

Pin	Signal Name	Function	In/Out
1	-HOST RESET	Reset signal from host	OUT
2	GND	Ground	OUT
3	HOST D7	Data bit 7	I/O
4	HOST D8	Data bit 8	I/O
5	HOST D6	Data bit 6	I/O
6	HOST D9	Data bit 9	I/O
7	HOST D5	Data bit 5	I/O
8	HOST D10	Data bit 10	I/O
9	HOST D4	Data bit 4	I/O
10	HOST D11	Data bit 11	I/O
11	HOST D3	Data bit 3	I/O
12	HOST D12	Data bit 12	I/O
13	HOST D2	Data bit 2	I/O
14	HOST D13	Data bit 13	I/O
15	HOST D1	Data bit 1	I/O
16	HOST D14	Data bit 14	I/O
17	HOST D0	Data bit 0	I/O
18	HOST D15	Data bit 15	I/O
19	GND	Ground	OUT
20	KEY	Keyed pin	N/C
21	RSVD	Reserved	N/C
22	GND	Ground	OUT
23	-HOST IOW	Write strobe	OUT
24	GND	Ground	OUT
25	-HOST IOR	Read strobe	OUT
26	GND	Ground	OUT
27	RSVD	Reserved	N/C
28	RSV	Reserved	N/C
29	RSVD	Reserved	N/C
30	GND	Ground	OUT
31	HOST IRQ14	Drive interrupt request	IN
32	RSVD	Reserved	N/C

Table 2–25. IDE Drive Interface Connector (J12) (continued)

Pin	Signal Name	Function	In/Out
33	HOST A1	Drive address 1	OUT
34	RSVD	Reserved	N/C
35	HOST AD0	Drive address 0	OUT
36	HOST AD2	Drive address 2	OUT
37	-HOST CS0	Chip select	OUT
38	-HOST CS1	Chip select	OUT
39	-HOST SLV/ACT	Drive active/drive slave	10K Pull-up
40	GND	Ground	OUT

Table 2–26. J12 Mating Connector

Connector Type	Mating Connector
Ribbon	3M 3417-7600
Discrete Wire	MOLEX Housing 22-55-2402 PIN 16-02-0103

IDE Interface Configuration

Use SETUP to specify the IDE hard disk drive type. Refer to the SETUP section later in this chapter for details.

If a drive type whose displayed parameters match the drive being used is not found use drive type 48 or 49. These permit manual entry of the drive parameters described in the documentation provided by the drive's manufacturer. Use drive type AUTO for all IDE drives. AUTO automatically configures the drive type parameters from information provided by the drive itself.

Compact Flash Solid-State Disk

The Little Board/486*e* connector J2 supports a Compact Flash device, a solid-state IDE hard-disk emulator. It acts as a removable hard-disk drive. You can format, read, and write the Compact Flash device much as you would a standard IDE drive.

Enabling the Drive

The Compact Flash interface emulates an IDE drive to the operating system. To use this feature, enable it using Setup. The Compact Flash interface takes up one of the positions of the primary IDE drive controller. If you enable the Compact Flash interface, you can only add one additional hard drive to the primary IDE controller.

Master/Slave Setting

The Compact Flash interface can be configured to emulate a master or slave IDE device in the system.

- To configure the drive as *master*, install a jumper on W3.
- To configure the drive as *slave*, remove the jumper on W3.

An IDE drive attached to the primary IDE controller must have the opposite setting.

Solid-State Disk Preparation

To prepare Compact Flash device for use in the system, insert the device in connector J2. Boot the system and prepare the drive just as you would a new IDE drive. That is, use the DOS FDISK utility to set up one or more partitions, and then use the DOS FORMAT utility to format the drive.

A Compact Flash device, properly formatted and programmed, can be used as a boot drive. To do so, you must configure the drive to be master by installing a jumper on W12. First FDISK the device as a primary DOS partition, then format the drive using the /S option to include the DOS operating system.

Flat Panel/CRT Video Controller

The Little Board/486*e* CPU provides an integrated high-performance super VGA video controller that supports both CRT and flat panel displays. Table 2–27 provides a summary of the Video Interface connectors and their specific use and features are described in the following sections.

It is possible to disable the on-board video controller by removing jumpers W11 and W12. This can help developers recover from a misprogrammed video BIOS by allowing the installation of a second display card. To re-enable the video controller, install W11 and W12 and reset the system.

Table 2–27. Video Connector Summary

Name	Connector	Pins/Type	Description
Flat Panel	J3	50-pin Shrouded .100 Header	Provides connections for a broad array of standard flat panel displays. Intended for standard 50-wire ribbon cable.
LCD Bias Supply Option	J4	12-pin Shrouded .100 Header	Ampro provides a small add-on board that will supply the Vee voltage for most common LCD flat panel displays. It mounts to this connector. For details about the Vee Supply Option, refer to it's section, below.
CRT	J5	10-pin Shrouded .100 Header	Provides connections for a CRT display. To connect to a standard CRT cable, use a short transition cable to a DB-15 connector.

Connecting a CRT (J5)

Analog video signals from the video controller appear on 10-pin dual row header, J5. These signals are compatible with the standard video monitors commonly used with desktop PCs. Specifications for compatible monitors are provided in Chapter 3.

Normally, signals from J5 are connected to a standard DB-15 video connector by a transition cable made from a ribbon cable connector and a short length of 10-wire ribbon cable. The transition cable can connect the video signals to a bulkhead-mounted DB-15 or DB-9 connector, allowing any standard CRT to be easily connected using a standard monitor video cable. Table 2–28 gives the signal pinout of J5 and pin connections for a DB-15 connector. Pin connections for a DB-9 connector, used for some monitors are also provided. Table 2–29 26 shows manufacturer's part numbers for mating connectors to J5.

Table 2–28. CRT Interface Connector (J5)

J5 Pin	Signal Name	DB-15	DB-9
1	Red	1	1
2	Ground	6	6
3	Green	2	2
4	Ground	7	7
5	Blue	3	3
6	Ground	8	8
7	Horizontal Sync.	13	4
8	Ground	10	9
9	Vertical Sync.	14	5
10	+5V Power with Fuse	_	_

Table 2–29. J5 Mating Connectors

Part Description	Mating Connector
Ribbon	3M 3473-7600
Discrete Wire	MOLEX Housing 22-55-2102 PIN 16-02-0103

Connecting a Flat Panel (J3)

Signals for a wide range of flat panel displays, both color and gray scale, appear on connector J3. Although flat panels of a similar type use similar sets of signals from the video controller, they do not share a standardized interface connector pin configuration. The names of panel control signals vary from manufacturer to manufacturer. Read the description of each signal carefully to determine how each signal is used for the display you choose. Refer to the panel manufacturer's technical literature to determine how to wire a cable for the panel you choose for your application.

Cable diagrams for Ampro-supported panels can be found on the Utilities diskette.

Jumper W10 is a 6-pin header that allows for selecting the proper voltage required by a particular panel, see Figure 2–8. Two jumper shunts are used to provide adequate current capacity. When jumpered 1/3 and 2/4, +5V is selected to power the panel. When jumpered 3/5 and 4/6, +3.3V is selected.

Figure 2–8. LCD Power Selector Configuration (W10)

Caution

Make sure that both jumper shunts are connected as illustrated in Figure 2–8 to avoid shorting the +5V and +3.3V power inputs.

Table 2–30 lists the signals available on connector J3. Table 2–31 shows manufacturer's part numbers for mating connectors to J3.

Table 2–30. Flat Panel Video Connector (J3)

Pin	Signal Name	Description
2, 34, 37	+5V	+5 Volt supply from the Little Board/486*e* CPU
3	+12V	+12 Volt supply from J10
5	ShfClk	Shift Clock. Pixel clock for flat panel data. Sometimes called Video Clock.
7	M	M signal for panel AC drive control. Sometimes called ACDCLK or AC Drive. May also be configured to be -BLANK or as Display Enable (DE) for TFT panels.
9	LP	Latch Pulse. Sometimes called Load Clock, Line Load, or Input Data Latch, the flat panel equivalent of HSYNC.
10	FLM	First Line Marker. Also called Frame Sync or Scan Start-up. Flat panel equivalent to VSYNC.
12 – 31	VD0 – VD19	Panel video data 0 through 19 (in order). For 8-, 9-, 12-, or 16-bit flat panels.
36	ENABKL	Enable backlight. Power control for panel backlight. Active High, same as ENAVEE.
38	ENAVEE	Enable Vee. Power sequencing control for panel bias voltage. Active high.
39	ENAVDD	Enable Vdd. Power sequencing control for panel driver electronics Vdd. Active high.
41	VD20	Video data 20
42	VD21	Video data 21
43	VD22	Video data 22
44	VDDSAFE	Swiched power supply to panel
45	VD23	Video data 23
46	VEE	Switched Vee supply to panel from LCD Bias Supply
47	EXTCONT	External contrast adjustment to LCD Bias Supply
50	+12VSAVE	Switched +12V supply to panel
1, 4, 6, 8, 40, 48, 49	Ground	Ground
11, 32, 33, 35	N/C	No connection

Table 2–31. J3 Mating Connectors

Part Description	Mating Connector
Ribbon	3M 4325-7600
Discrete Wire	MOLEX Housing 55-22-2502 PIN 16-02-0103

Power Sequencing

Some LCD panels can be damaged when the Vee bias supply is applied to the LCD substrate without first enabling the control and data lines. This can result in damage to the panel or reduction of its operational life. The video controller generates signals for sequencing the power in the proper order to protect the panel from these effects. If an external power supply is connected, special enabling signals ENVEE and ENVDD provided on the J3 connector must be used to enable this supply.

As an option, Ampro provides a Vee bias supply board that will interface to the Little Board/486*e* CPU through connector J4. This board contains circuitry to generate a Vee bias voltage that is already properly sequenced.

Advanced Power Management

The same signals that support power sequencing also provide for power management. On-board circuitry provides the following power management features in *panel off mode*:

- CRT - OFF
- FPD – OFF
- VGA subsystem registers and display memory - ON

In *standby mode*, the following occurs:

- CRT – OFF
- FPD Interface – OFF
- VGA Subsystem – OFF
- Screen DRAM – Low power mode (only DRAM is refreshed)

BIOS Support of Non-Standard Panels

Ampro supplies flat panel BIOS images for many popular LCD panels. The chosen panel BIOS is selected using SETUP. If an unsupported panel is desired, the standard video BIOS must be modified to support the panel. Ampro can provide a BIOS modification kit to make these changes. Contact an Ampro sales representative or Ampro Technical Support for information about the Little Board/486*e* Flat Panel BIOS Modification Kit.

Once you have modified a BIOS, you must load it into the video BIOS section of an onboard Flash EPROM device (already on the Little Board/486*e* CPU). Ampro provides a Flash programming utility to do this.

To install a new video BIOS, follow this procedure:

1. Remove EMM386, HIMEM, and other extended memory managers from your CONFIG.SYS or AUTOEXEC.BAT files. No extended memory managers can be loaded. (You must reboot the system for these changes to take effect.) Alternately, boot the system from a floppy that has no memory managers installed.
2. Remove the jumper on W1 to enable programming.
3. Enter the following command on the DOS command line:

   `PGMEBIOS VIDEO=`*`filename`*

   where *`filename`* is the name of the new video BIOS code file. (Frame the command so that DOS accesses PGMEBIOS wherever it resides on your system.)

   Leading and trailing spaces around the “=” are ***not*** allowed.

   PGMEBIOS will return to the prompt indicating when programming is complete. DO NOT REBOOT!
4. DO NOT remove power. Restore jumper W1.
5. Reboot the system and test the result.

LCD Bias Supply Option

The LCD Bias supply option is a small circuit board that supplies Vee power to an LCD display. The board converts the +5V from the Little Board/486*e* CPU to the Vee voltage (between 15V – 35V) required by many LCD panels. This voltage is available on flat panel connector J3.

LCD displays are sensitive to the sequence order and timing that power supply and control signals are applied to the display during power up and removed during power down cycles. LCD manufactures warn OEMs that violating the sequence and timing specifications of these signals can damage the display or reduce its service life. The LCD Bias supply option, in conjunction with control signals from the Little Board/486*e* video controller automatically sequences the appropriate signals to meet the requirements of virtually any LCD display

The Ampro LCD Bias Supply option mounts parallel to the Little Board/486*e* CPU connected to the board via a 12-pin connector, J4. Secure the board to the Little Board/486*e* CPU using a .6 inch standoff. Table 2–32 shows the connector pinout for J4, with a description of each signal. Some signals also appear on flat panel connector J3.

Table 2–32. LCD Bias Supply Option Connector (J4)

J4 Pin	J3 Pin	Description
1		Ground
2		+5V to the Vee Supply Option Board
4		Ground
6	38	Enable Vee TTL control signal driver by the VGA controller chip
8		Ground
11	46	Vee output, to panel
12	47	Contrast adjustment Analog control signal

Selecting Vee Polarity

Most LCD displays require a Vee supply of between 15v – 35V. Some panels need a negative supply, and some a positive supply. The LCD Bias Supply Option provides a jumper for selecting the Vee output polarity. To select the polarity for the panel being used, set the jumper on W1 on the LCD Bias Supply board, not on the Little Board/486*e* CPU, as shown in Figure 2–-9.

Figure 2–9. Vee Polarity Selection Jumper

Note

Incorrect Vee polarity or voltage can damage an LCD panel. Set the polarity and voltage on the Vee supply before connecting the LCD panel.

Attaching an External Contrast Control

Vee controls the contrast of the LCD display. Do not confuse this with a backlight that illuminates the screen using one or more fluorescent tubes. Backlights generally require a high voltage AC supply.

An onboard control (R1) allows you to set the precise Vee voltage for the contrast you require. However, you may want to provide a more accessible Vee control so that the user can set the display contrast to accommodate various ambient lighting conditions. The board provides a jumper and control signal to allow the attachment of a remote potentiometer.

To use the contrast potentiometer on the LCD Bias Supply board, install a jumper on W2 (on the LCD Bias Supply board).

To use an external potentiometer, remove the jumper from W2, and attach the circuit shown in Figure 2–10 between J3-47 and ground.

Figure 2–10. External Contrast Adjustment for LCD Panels

Select Ra and Rb to provide the appropriate voltage range adjustment for the LCD panel you are using. Consult your panel's technical literature for the range of voltages you need to supply for contrast adjustment. Use the following formulae to calculate the resistor values (in K Ohms).

$$Ra = \frac{270}{(Vee\ max / 1.5) - 1} - 12 \qquad Rb = \frac{270}{(Vee\ min / 1.5) - 1} - 12 - Ra$$

Example:

Suppose the following Vee values are shown in the panel's data sheet:

Vee max = 24V

Vee min = 20V

Calculate the required resistor values as follows:

Ra = (270 / (24 / 1.5) –1) –12

Ra = 6K ohms

Rb = (270 / (20 / 1.5) –1) –12 –6

Rb = 3.9K ohms

Ethernet Network Interface

This section discusses the hardware and software considerations when setting up a network using the Ethernet LAN interface. Additional information on Ethernet standards is available from IEEE Customer Service:

IEEE Customer Service
445 Hoes Lane
PO Box 1331
Piscataway, NJ 08855-1331 USA
Phone: (800) 678-IEEE (in the US and Canada)
(908) 981-0060 (outside the US and Canada)
FAX: (908) 981-9667
www.uncoverco.com/CUSTSR.HTM

There are no jumpers to set on the Ethernet interface, and no hardware configuration, other than connecting the network cable to an appropriate connector. Software configuration of the Ethernet interface is included in the utility disks.

Network Terms

The following are some of the terms used in this section:

- **Trunk or network segment**—The cable over which network stations communicate. A segment cable is usually made up of several cable lengths connected together. A segment is limited in its total length and the number of network stations it can support. However, a network is not limited to one segment.
- **Network trunk** —The sum of all the segment cables. Several segments can be interconnected with repeaters, routers, or bridges to form the network trunk cable.
- **Repeater**, router, or bridge—Devices that extend the size of a network beyond the limitations of one segment. These devices not only form a pathway for network signals traveling from one trunk segment to another; they also regenerate and strengthen network signals.
- **Station**—Any device that is connected to a network by means of a network interface card; e.g., the Little Board/486*e* CPU.
- **Node**—Another term for a network station. Each node has its own network interface card.
- **Attachment Unit Interface**—(AUI) One of the standard interfaces used to connect a node to the net, often used between a network interface card and a hub or concentrator.

Installing an Ethernet Boot PROM

Most network interface cards provide a means for installing a boot PROM. The boot PROM code enables the node to boot from a network server, much like the BIOS boots from a local hard disk or floppy. Install this device in S0.

Boot PROM code varies from one network operating system to another. Boot PROM for the selected network operating system must be compatible with the onboard LAN controller. Boot PROMs are available from LanWorks for:

- Novell Netware
- Microsoft LAN Manager
- QNX
- Other popular network operating system providers.

Contact LanWorks at the following address for information about their bootware:

LanWorks Technologies Inc.
2425 Skymark Ave.
Mississauga, Ontario, Canada
Phone: 800-808-3000
905-238-5528
FAX: 905-2238-9407
E-mail: sales@mhs.lanworks.com
www.3com.com/lanworks

Addresses and phone numbers of companies providing compatible LAN drivers:

Novell, Inc.
1640-D Berryessa Rd.
San Jose, CA 95133
Phone: 408-729-6700
www.novell.com

Microsoft Corporation
One Microsoft Way
Redmond, WA 98052-6399
Phone: 800 426-9400
www.microsoft.com

QNX Software Systems
175 Terrence Matthews Cr.
Kanata, ON K2M 1W8
CANADA
Phone: 613-591-0931
FAX: 613-591-3579
www.qnx.com

Installing a Boot PROM

The Little Board/486*e* CPU can be configured for a boot PROM by installing the boot PROM in byte-wide socket S0.

Installing a Boot PROM in Byte-Wide Socket S0

Install a LAN boot PROM in byte-wide socket S0. The boot PROM code is run at boot time as a BIOS extension.

To install a LAN boot PROM in byte-wide socket S0, follow these guidelines:

1. Either obtain a preprogrammed boot PROM device, or program a PROM or FLASH EPROM with the boot PROM image. Use a 128K byte device, such as a 27C010, if possible.
2. Install the boot PROM device in S0.
3. In SETUP, set socket S0 for 64K bytes at D0000h and select S0 to be enabled at boot time.

Twisted Pair Interface (J7)

The twisted pair interface (10BaseT) appears on connector J7. It is a standard RJ45 telephone-type modular connector, which is the normal connector used with standard twisted-pair cables. Table 2–33 lists the signals and pin numbers of J7.

Table 2–33. RJ45 Twisted Pair Connector (J7)

J7 Pin	Function
1	+ Transmit Data
2	- Transmit Data
3	+ Receive Data
4	N/C
5	N/C
6	- Receive Data

Twisted-Pair Installations

This section discusses the guidelines for twisted-pair installations.

- Connector jack—A standard RJ45-terminated cable can be plugged directly to the female RJ45 connector on the Little Board/486*e* CPU.
- Connector plug—The RJ45 connector plugs attach to both ends of twisted-pair Ethernet cable lengths. They are used to connect the Little Board/486*e* CPU to a hub or concentrator.
- Terminators—There are no external termination devices required. Termination is handled automatically by the hub devices.

Twisted-pair Ethernet cable is 22 or 24 gauge copper wire twisted together in pairs. Ethernet twisted-pair uses two pairs (four wires), one for transmitting and one to receive. It is available from

many industry suppliers. Standard RJ45 connectors are used for all connections in a twisted-pair cable network. Twisted-pair Ethernet cables must be 100 meters or less between any node and hub or repeater.

Using Network Operating Systems (NOS)

The most common method of using the Little Board/486*e* Ethernet LAN interface is by means of a NOS. The NOS can be either part of the computer's OS; DOS and Windows 9x, or provided separately.

Novel Netware's NOS supports client server communication; a central computer that runs Netware as its NOS provides file server and network services to the distributed systems connected to the LAN. Each node on the network must also have a compatible NOS installed.

Modern network architectures are based on the Open Standards Interconnect (OSI) model that defines:

- Layers of software between the network hardware
- Network operating system
- Applications that use the network services

At the bottom level is the actual Ethernet cable and the hardware interface, in this case, the Little Board/486*e* LAN interface. A driver talks directly with the hardware, masking any unique differences in the hardware from the layers above it, including the NOSs. Several NOS drivers compatible with the Little Board/486*e*'s LAN hardware are provided on the Utilities diskette that is included with Little Board/486*e* Development Kit. New drivers or new versions of existing drivers are made available on Ampro's Technical Support bulletin board. The driver is the only unique software needed to use the LAN interface. The supported NOSs provide the other layers in the OSI model.

Network OS Drivers

Ethernet drivers provided on the Utilities diskette are listed in Table 2–34. The table which driver to use for various NOSs.

Driver installation procedures vary from one network operating system to another. No detailed description can be given here. Follow the instructions that come with the network operating system you choose for your system.

Table 2–34. Ethernet Drivers

Program Name	Vendor	Function	Driver Name
Netware 4.1 Server Driver	Novell	ODI on server	SMC9000.LAN
Netware 3.11 Server Driver	Novell	ODI on server	SMC9000.LAN
Netware 2.2 Server Driver	Novell	IPX on server	SMC9000.LAN
Netware ODI Workstation Driver	Novell	ODI on workstation	SMC9000.COM
OS/2 ODI Workstation Requester	Novell	ODI on workstation	SMC9000.SYS
LAN Manager	Microsoft	NDIS for DOS	SMC9000.DOS
LAN Manager	Microsoft	NDIS on Windows for Workgroups	SMC9000.DOS
LAN Manager	Microsoft	NDIS for Windows NT 3.1 and NT 3.5	SMC9000.SYS
LAN Manager	Microsoft	NDIS for OS/2 on server	SMC9000.OS2

Controlling the Ethernet LAN Interface Directly

Of course, you can create any application or software driver to directly control the SMC Ethernet controller chip used on the Little Board/486*e* CPU. Ampro has designed the interface to conform to the standards and recommendations set forth by the controller chip manufacturer. To develop a custom driver, you need detailed information on the SMC9000-series controller chip, which is available from SMC. Contact SMC at the following address:

SMC
80 Arkay Drive
Hauppauge, NY 11788
Phone: (516) 435-6000
FAX: (516) 231-6004
www.smc.ru

Manufacturer's Ethernet ID

Ethernet network adapter and interface manufacturers are assigned a unique manufacturer's ID by the IEEE Standards Office. A network address consists of 48 bits. The upper 24 bits are the manufacturer's ID and the lower 24 bits are the board's unique ID.

Developers creating network applications must know whether the manufacturer's ID for network adapters attached to the network are important or not.

Ampro's 24-bit manufacturer's ID for Ethernet controllers is displayed in hex as follows:

00 40 53

Ethernet IDs are sometimes displayed by diagnostic or network analysis programs in binary format. Refer to your equipment manual for information on possible byte swapping in the display, as shown in this example.

1010 1100 0010 0000 0000 0000

Byte-Wide Socket (S0)

The Little Board/486*e* CPU has a 32-pin onboard byte-wide memory socket designated **S0**. This socket supports 32-pin DIP JEDEC pin out memory devices, including EPROM, FLASH EPROM, SRAM, and nonvolatile RAM (NOVRAM) devices.

A memory device installed in the byte-wide socket can be used for:

- Simple program storage
- BIOS extension
- Solid State Disk (SDD)

Table 2–35 shows representative byte-wide memory devices that can be installed in the byte-wide socket. The table gives examples of generic part numbers, the size of the device (K bytes), and the DIP package pin count. It also lists the SSD device type, used by the Ampro Solid State Disk (SSD) Support Software to identify memory devices.

Table 2–35. Typical Byte-wide Devices

SSD Device Type	Size	Package Pins	Generic Part Number
EPROM			
EPROM128	128K byte	32	27C010
EPROM256	256K byte	32	27C020
EPROM512	512K byte	32	27C040
EPROM1024	1024K byte	32	27C080
Flash EPROM			
EPROM128	128K bytes	32	28F010
EPROM256	256K bytes	32	28F020
EPROM512	512K bytes	32	29F040
SRAM			
SRAM128	128K bytes	32	62204
SRAM512	512K bytes	32	434000

Addressing the Byte-wide Socket

Use SETUP to specify the size and starting address of the byte-wide socket, and whether the BIOS enables the socket upon system initialization. Table 2–36 lists the possible settings for sizes and address ranges of the byte-wide socket.

Note

When the byte-wide socket is enabled, the memory address space it uses is unavailable for other devices, even if no memory device is installed in the socket. You must disable the byte-wide socket in SETUP before you can use the memory space for other purposes.

Table 2–36. Window Size and Address Selection

Window	Address
DISABLE	N/A
64K	D0000-DFFFFh
64K	E0000-EFFFFh
128K	D0000-EFFFFh

A device used in the byte-wide socket must have access times of 250 nS or less.

If you install a device that is smaller than the selected window size, the contents of the device are duplicated in the byte-wide socket's memory space. For example, the software sees two copies of a 32K device in a 64K window, and 4 copies in a 128K window.

A16 is inverted so 128K devices programmed off board will have the halves swapped, for example, the lower half will be in the E0000 segment.

ROM-BIOS Extensions

The system can be configured to run its application from the byte-wide socket instead of loading it from a disk drive. This technique, known as a ROM BIOS extension, directly executes the application during the Power-On Self Test (POST) instead of booting from floppy or hard disk. For additional information regarding the ROM-BIOS extension concept and its practical implementation, contact Ampro Technical Support.

Performance Issues

Executing programs directly from the byte-wide socket can adversely affect system performance. There are a number of factors that can contribute to the performance impact:

- The byte-wide device is substantially slower than DRAM, as it is an 8-bit device instead of 32-bit device.
- The device is accessed from the PC expansion bus, which is much slower than the high-speed processor memory bus.

Performance can be substantially improved by copying the contents of the byte-wide device into RAM and executing directly from RAM.

Solid State Disk (SSD) Drives

Using the Ampro Solid State Disk (SSD) Support Software, you can configure EPROM, Flash EPROM, or SRAM solid-state devices, installed in the byte-wide sockets, to act as one or more disk drives. No custom programming is required. Regular DOS-compliant programs, including standard DOS utilities, can be used without modification.

Ampro's SSD support software creates data image files, based on your application programs and operating system, which can be programmed into the devices you install in the byte-wide sockets. The Ampro ROM-BIOS treats these devices like one or more disk drives, loading the programs into DRAM for execution. The sockets can be combined to serve as a single drive, or each socket can be used as a separate drive. You can use SSD drives in addition to, or instead of, normal floppy and hard disk drives.

You can increase system SSD capacity by adding one or more of Ampro's SSD expansion modules.

Accessing the Byte-Wide Socket

To access the byte-wide socket, it must be enabled. Using SETUP, either device can be enabled at boot time. This places the contents of the enabled device at the address specified in SETUP and the processor can access this memory in a normal fashion.

Here is a simple assembly language routine showing how to use an Ampro extended-BIOS call to enable or disable the byte-wide memory socket, S0. This code selects the first 64K page on large devices.

```
;-------------------------------------------------------
; Access control code for a byte-wide socket
;-------------------------------------------------------
MOV   AH,0CDH                ; AMPRO function call
MOV   AL,03h                 ; Use 03 for S0
MOV   BL,nn                  ; Use 01 to turn ON or 00 to turn OFF
MOV   BH,00                  ; Selects page 0 of the device
INT   13H
```

Table 2–37 lists the segment addressing in large memory devices.

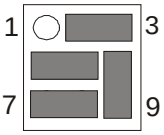
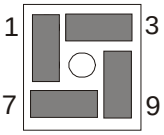
Table 2–37. Segment Addressing in Large Memory Devices

Device Size	64KB Segments	Segment Address (Upper Nibble of BH)	
128K	2	FIRST SECOND	BH=00h BH=10h
256K	4	FIRST SECOND THIRD FOURTH	BH=00h BH=10h BH=20h BH=30h
512K	8	FIRST SECOND THIRD FOURTH FIFTH SIXTH SEVENTH EIGHTH	BH=00h BH=10h BH=20h BH=30h BH=40h BH=50h BH=60h BH=70h
1M	16	FIRST SECOND THIRD FOURTH FIFTH SIXTH SEVENTH EIGHTH NINTH TENTH ELEVENTH TWELFTH THIRTEENTH FOURTEENTH FIFTEENTH SIXTEENTH	BH=00h BH=10h BH=20h BH=30h BH=40h BH=50h BH=60h BH=70h BH=80h BH=90h BH=A0h BH=B0h BH=C0h BH=D0h BH=E0h BH=F0h
Note: For a 128K byte window, use any of the odd numbered values (for instance, FIRST or THIRD)			

Jumpering the Byte-Wide Socket

You must jumper the byte-wide socket for the devices you install. Jumper array W2 configures S0 for a particular device type. Table 2–38 shows how to install jumpers for supported memory devices.

Table 2–38. EPROM Jumpering for S0 (W2)

EPROM Typical Devices	Pins	Jumper Diagram
128K EPROM - 27C010 256K EPROM - 27C020	32	
512K EPROM - 27C040 1M EPROM - 27C080	32	

Byte-Wide Socket Signals

A jumper W2 for S0, configures the byte-wide sockets for specific memory devices. Table 2–39 lists the signals that appear on the pins of W2.

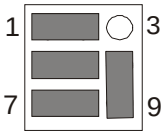
Table 2–39. Byte-Wide Jumper Pin Signals (W2)

W14 Pin	Signal Name	Description
1	A18	Address A18 (static)
2	Pin 1	Connection to pin 1 of the byte-wide socket
3	A19	Address A19 (static)
4	Pin 31	Connection to pin 31 of the byte-wide socket
5	-SMEMW	Write strobe
6	Pin 29	Connection to pin 29 of the byte-wide socket
7	A15	Address SA15 from the expansion bus
8	Pin 3	Connection to pin 3 of the byte-wide socket
9	A14	Address SA14 from the expansion bus

Using EPROMs

)If you install an EPROM in socket S0, make sure the jumper on W2 is set properly. Some EPROMs draw current through their chip select lines (or other pins) when powered down. Table 2–40 lists the Flash EPROM jumpering for S0.

Table 2–40. Flash EPROM Jumpering for S0

Flash EPROM Typical Devices	Pins	Jumper Diagram
128K 5V Flash EPROM - 29F010 256K 5V Flash EPROM - 29F020 512K 5V Flash EPROM - 29F040	32	

FLASH EPROM Programming

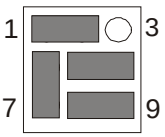
To program a Flash device in byte-wide socket S0, use the FlashWRI.EXE utility supplied on the Common Utilities diskette. The Common Utilities manual describes its operation. Only devices with 5V programming power are supported.

Custom Flash-programming routines can be developed using extended BIOS calls in the ROM BIOS. Contact Ampro Technical Support for information about the extended BIOS call provided for Flash programming power.

Using SRAMs

The external battery power is combined with the internal battery using low forward voltage drop Schottky diodes. Table 2–41 lists the SRAM and NOVRAM jumpering for S0.

Table 2–41. SRAM and NOVRAM Jumpering for S0

SRAM Typical Devices	Pins	Jumper Diagram
128K SRAM - 628128 512K SRAM - 628512	32	

Non-volatile RAM

Non-volatile RAM can be used as a means of dramatically storing and retrieving runtime application data. NOVRAM has the following specifications:

- 32 pin
- 128K bytes maximum in segments D0000 and E0000
- Must be programmed in place on the Little Board/486*e* CPU
- NOVRAM offers some advantages over Flash EPROM including faster access speeds and unlimited write operations.

Utility Connector (J16)

10 functions appear on the 16-pin connector at J16:

- Auxiliary power connections
- Power indicator LED
- PC speaker
- Push-button reset switch
- Standard PC keyboard interface
- External back-up battery for the real-time clock

Table 2–42 shows the pinout and signal definitions of the Utility Connector. Since there are connections for diverse features on this single connector, a discrete-wire connector should typically be selected rather than a ribbon cable connector, although this is not a requirement. Table 2–43 shows manufacturer's part numbers for both types of mating connectors.

Table 2–42. Utility Connector (J16)

Pin	Signal Name	Function
1	-12V power	Connect external –12V supply here for distribution to expansion cards needing this voltage
2	Ground	Ground return
3	-5V power	Connect external –5V supply here for distribution to expansion cards needing this voltage
4	Ground	Ground return
5	LED Anode	LED current source (+5V through 330 ohms)
6	EXSMI	External SMI
7	Speaker +	PC audio signal output
8	Ground	Ground
9	Reset	To one side of the manual reset button
10	N/C	No connection
11	Kbd Data	Keyboard serial data
12	Kbd Clk	Keyboard Clock
13	Ground	Keyboard ground
14	Kbd Power	Keyboard +5V power
15	BATV +	External battery +
16	BATV-	External battery -

Table 2–43. J16 Mating Connector

Connector Type	Mating Connector
Ribbon	3M 3452-7600
Discrete Wire	MOLEX Housing 22-55-2162 Pin 16-02-0103

PC Speaker

The Little Board's motherboard logic includes a standard AT-compatible speaker port. The speaker logic signal is buffered by a transistor amplifier, and provides about 100 mW on J16-9 to an external 8-ohm speaker. Connect the other side of the speaker to ground, J16-10.

The audio output is based on two signals: the output of Timer 2; and the programming of two bits, 0 and 1, at I/O port 61h. Bit 1 of I/O port 61h is one term of a 2-input AND gate. The other term is the output from Timer 2. Thus, setting bit 1 to logic 1 enables the output of Timer 2 to the speaker, and logic 0 disables it. Disabling Timer 2 by setting bit 0 of port 61h to a 0 causes its output to go high. Then, use bit 1 of port 61h to control the speaker directly.

LED Connection

To connect an external LED power-on indication lamp, connect the LED anode (-) to J16-7 and the cathode (+) to ground. J16-7 provides +5V through a 300 ohm resistor.

Push Button Reset Connection

J16-1 provides a connection for an external normally open momentary switch to manually reset the system. Connect the other side of the switch to ground. The reset signal is "de-bounced" on the board.

Keyboard Connections

An AT (not PC) keyboard can be connected to the keyboard port. J16-13 through J16-16 provide this function. Normally, AT keyboards include a cable that terminates in a male 5-pin DIN plug for connection to an AT. Table 2–44 lists the keyboard connector pinout and signal definitions, and includes corresponding pin numbers of a normal AT DIN keyboard connector.

Table 2–44. Keyboard Connector (J16)

J16 Pin	Signal Name	DIN Pin
14	Keyboard Clock	1
13	Keyboard Data	2
N/C	No connection	3
15	Ground	4
16	Keyboard power	5

External Battery Connections

To connect an external battery, connect its positive terminal to J16-17 and its negative terminal to J16-18. Use a 3.6-volt lithium cell.

The battery is connected by a low-drop Schottky diode. Two blocking devices are in series with the battery, complying with UL recommendations for lithium batteries.

Battery-Backed Clock

An AT-compatible battery-backed real-time clock (with CMOS RAM) is standard on the Little Board/486*e* CPU. A 3.6-volt Lithium battery connected to the Utility Connector, J16, can power the clock. Battery drain for the clock is less than 1 uA. This battery will support the clock for about 10 years.

Use the Ampro SETUP utility to set the current time and date in the real-time clock, as well as SETUP information in the CMOS RAM portion of the clock chip (configuration memory).

The contents of the configuration memory are also stored in an onboard EEPROM. The ROM BIOS reads the EEPROM to get configuration information if the CMOS RAM data is lost. This means that the board functions without the battery. However, without a battery the real-time clock date and time will not be correct.

Watchdog Timer

The purpose of a watchdog timer is to restart the system should some mishap occur. Possible problems include:

- A failure to boot properly
- Application software losing control
- Temporary power supply problems including spikes, surges, or interference
- Failure of an interface device
- Unexpected conditions on the bus
- Other hardware or software malfunctions

The watchdog timer helps assure proper start-up after any interruption.

The Little Board/486*e* ROM BIOS supports the board's watchdog timer function in two ways:

- There is an initial watchdog timer setting, specified using SETUP, which determines whether the watchdog timer is used to monitor the system boot, and if so, the length of the timeout. The options are Disable, 30 seconds, 60 seconds, and 90 seconds.
- There is a standard ROM-BIOS function that can be used by application software to start, stop, and retrigger the watchdog timer function.

The initial time-out should be set using SETUP to be long enough to guarantee that the system can boot and pass control to the application. Once the system is booted and the application is running, the application must periodically retrigger the timer so that a watchdog timer time-out does not occur. If the time-out does occur, the system responds in a manner determined by how the watchdog timer jumper, W4, is set. See Figure 2–11.

Figure 2–11. Watchdog Timer Response Jumper (W4)

The watchdog timer uses the standard alarm feature of the real-time clock. In a standard AT, the alarm output is connected to IRQ8. On the Little Board/486*e* CPU you can also jumper the alarm output to I/O Channel Check (-IOCHCK) or RESET with W4. I/O Channel Check is the bus signal that triggers a non-maskable interrupt (NMI). RESET is a hard reset signal, the same as pressing the Reset button. Watchdog timer responses are summarized in Table 2–45.

Table 2–45. Watchdog Timer Setup

Jumper W4	SETUP	WDT Response
W4-1/2 Shorted	Enabled	I/O Channel Check (NMI)
W4-2/3 Shorted	Enabled	Hardware Reset
W4 Open	Enabled	IRQ8 turns off interrupt. System continues unaffected
W4 Open	Disabled	No action

Note

If you use the MS-DOS operating system, you cannot use the watchdog timer to monitor the boot process. MS-DOS resets the alarm clock in the real-time clock at boot time.

The following assembly language routine illustrates how to reset the watchdog timer using the standard PC BIOS function call:

```
;---------------------------------------------------------
; Watchdog timer control program
;---------------------------------------------------------
MOV   AH,0C3h                ; Watchdog Timer BIOS function
MOV   AL,nn                  ; Use “00” to disable; “01” to enable
                             ; timer.
MOV   BX,mm                  ; Selects time, in seconds
                             ; (00-FFh; 1-255 seconds)
INT   15h
```

Ampro provides a simple DOS program that can be used from the command line or in a batch program to manage the watchdog timer. It is called WATCHDOG, and is described in the Ampro Common Utilities manual.

Note

Some versions of DOS turn off the real-time clock alarm at boot time. If your DOS does this, make sure that your application program enables the alarm function using this BIOS call.

If the output of the Watchdog Timer is jumpered to trigger a non-maskable interrupt (NMI), an NMI IO Channel Check is asserted by the real-time clock alarm circuit when it times out. For the system to respond to the NMI, the NMI circuit must be enabled. (In the PC architecture, the non-maskable interrupt can be masked.) To enable (unmask) the NMI, execute the following code.

```
;-------------------------------------------------
; To enable NMI (IO channel check)
;-------------------------------------------------
IN    AL,61H
AND   AL,NOT 08H
OUT   61H,AL
;-------------------------------------------------
```

To use the NMI I/O Channel Check in a custom Watchdog Timer handler routine, the standard NMI handler would have to be replaced with your custom code. If a customer supplied NMI interrupt service routine is installed, it can test to see if the I/O Channel Check NMI occurred by reading I/O port 61h, bit 6. Bit 6 is true (1) if the NMI occurred.

Note

Following the occurrence of an I/O Channel Check NMI, the function must be disabled and then re-enabled before the next one can occur.

The Watchdog timer is not compatible with Windows or other operating systems.

AT Expansion Bus

The PC/AT expansion bus appears on a pair of header connectors at P1 and P2. P1 is a 64-pin female dual-row header. P2 is a 40-pin female dual-row header. Pins from both headers extend through the board, providing male connections for PC/104-compliant peripherals or other devices.

The PC-bus subset of the expansion bus connects to the first 62 positions of P1; the two additional positions of P1 (A32 and B32) are added grounds to enhance system reliability. Connector P2 replaces the 36-pin edge card connector of a conventional ISA expansion bus. It has extra ground positions at each end of the connector (C0, D0, and D19). (C19 is a key pin.) The extra grounds C0 and D0 are numbered “0” to keep the pin numbers of the remaining signals on the connector the same as those on the standard ISA bus. The layout of signals on P1 and P2 is compliant with the PC/104 bus specification. PC/104-compatible expansion modules can be installed on the Little Board/486*e* expansion bus.

The buffered output signals to the expansion bus are standard TTL level signals. All inputs to the Little Board/486*e* CPU operate at TTL levels and present a typical CMOS load to the expansion bus. The current ratings for most output signals driving the AT expansion bus are shown in Table 2–46 through Table 2–49, and indicate how the signals are terminated on the Little Board/486*e* CPU.

Onboard MiniModule Expansion

One or more Ampro MiniModule products or other PC/104 modules can be installed on the Little Board/486*e* expansion connectors. When installed on P1 and P2, the expansion modules fit within the Little Board/486*e*'s outline dimensions. Most Ampro MiniModule products have stackthrough connectors compatible with the PC/104 Version 2.1 specification. Several modules can be stacked on the Little Board/486*e* headers. Each additional module increases the thickness of the package by 0.66 inches (15 mm). See Figure 2–12.

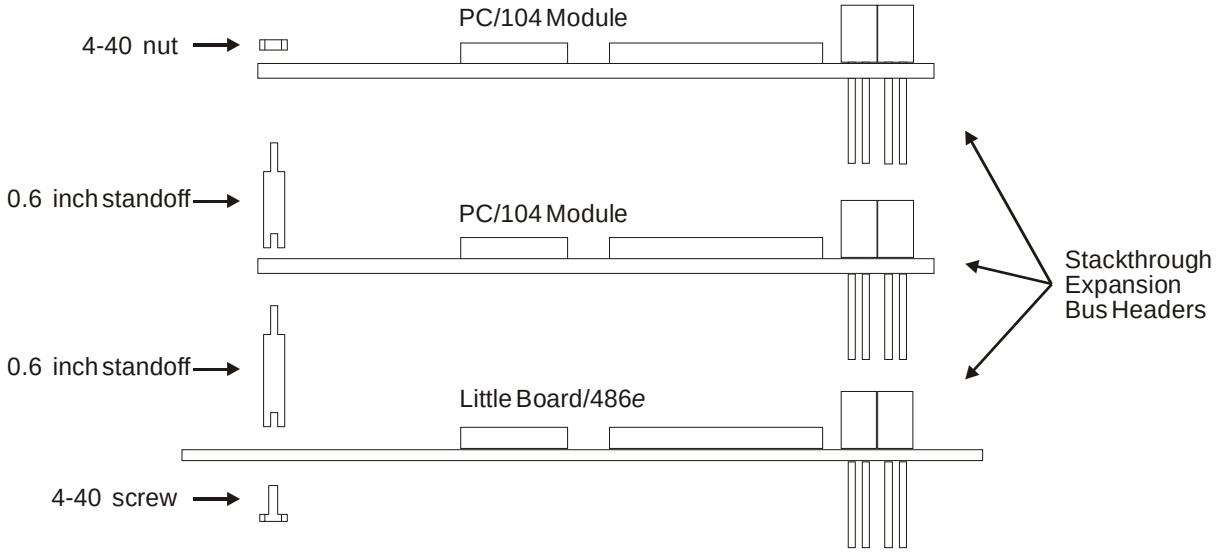


Figure 2–12. Stacking PC/104 Modules with the Little Board/486e CPU

Using Standard PC and AT Bus Cards

Since the PC/104 bus is electrically identical to ISA, it is also possible to attach conventional 8-bit and 16-bit ISA expansion cards to the Little Board/486*e* CPU. This requires some type of passive adapter to perform the physical transition from PC/104 bus headers to standard ISA slots. Contact Ampro to use conventional ISA expansion cards in Little Board/486*e* systems.

Bus Expansion Guidelines

Expanding a Little Board/486*e* CPU can be accomplished by connecting short ribbon cables to the header connectors. There are restrictions when attaching peripherals to the expansion bus with ribbon cables. If cables are too long or improperly terminated, noise and cross talk introduced by the ribbon cables can cause errors. Ampro strongly recommends conformance to the following guidelines:

- **Cable Length** and **Quality**—In general, the bus expansion cable must be as short as possible. Long cables reduce system reliability.

  For cables up to 6 inches, use a high quality standard cable, such as 3M 3365/64 (64 conductor) and 3365/40 (40 conductor).

  For cables between 6 and 12 inches long, use a high quality ground plane cable, such as 3M part number 3353/64 (64 conductor) and 3353/40 (40 conductor).

  Do not use cables over 12 inches long.

- **Backplane Quality**—If a backplane can be connected to the Little Board/486*e* CPU, use a high quality backplane that minimizes signal crosstalk. Use a backplane that has power and ground planes between trace layers, and run guard traces between sensitive bus signals.
- **Eliminating Reset and TC Noise**—Many cards have asynchronous TTL logic inputs that are susceptible to noise and crosstalk. The active high RESET and TC bus lines are especially vulnerable. These signals can be made more reliable by adding a 200 pF to 500-pF capacitor between the signal and ground to prevent false triggering by filtering noise on the signals.

Bus Termination

Some backplanes include bus termination to improve system reliability by matching backplane impedance to the rest of the system. The specification recommends the use of AC termination sometimes called *snubbers*, rather than resistive termination. The recommended AC termination is a 50 to 100 pF capacitor, in series with a 50 to 100 ohm resistor, from each signal to ground.

Caution

Do not use resistive bus termination! If the signal requires termination, use AC termination only.

The actual requirements for signal termination depend on system configuration, interconnecting bus cable and on the number and type of expansion modules used. It is the system engineer's responsibility to determine the need for termination.

Expansion Bus Connector Pinouts

Tables 2–34 through 2–37 show the pinout and signal functions on the PC/104-compliant expansion bus connectors. The expansion bus pin numbers shown in the following tables correspond to the scheme normally used on ISA expansion bus card sockets. Rather than numerical designations (1, 2, 3) they have alphanumeric designations (A1, A2..., B1, B2..., etc.).

The Little Board/486*e* CPU does not generate ±12VDC or -5VDC for the expansion bus. If devices on the bus require these voltages, they can be supplied to the bus connector from the Power Connector (J7).

Table 2–46. AT Expansion Bus Connector, A1-A32 (P1)

Pin	Signal Name	Function	In/Out	Current	PU/PD/S *
A1	IOCHCK*	bus NMI input	IN	N/A	
A2	SD7	Data bit 7	I/O	4 mA	4.7K PU
A3	SD6	Data bit 6	I/O	4 mA	4.7K PU
A4	SD5	Data bit 5	I/O	4 mA	4.7K PU
A5	SD4	Data bit 4	I/O	4 mA	4.7K PU
A6	SD3	Data bit 3	I/O	4 mA	4.7K PU
A7	SD2	Data bit 2	I/O	4 mA	4.7K PU
A8	SD1	Data bit 1	I/O	4 mA	4.7K PU
A9	SD0	Data bit 0	I/O	4 mA	4.7K PU
A10	IOCHRDY	Processor Ready Ctrl	IN	N/A	1K PU
A11	AEN	Address Enable	I/O	4 mA	
A12	SA19	Address bit 19	I/O	12 mA	
A13	SA18	Address bit 18	I/O	12 mA	
A14	SA17	Address bit 17	I/O	12 mA	
A15	SA16	Address bit 16	I/O	4 mA	
A16	SA15	Address bit 15	I/O	4 mA	
A17	SA14	Address bit 14	I/O	4 mA	
A18	SA13	Address bit 13	I/O	4 mA	
A19	SA12	Address bit 12	I/O	4 mA	
A20	SA11	Address bit 11	I/O	4 mA	
A21	SA10	Address bit 10	I/O	4 mA	
A22	SA9	Address bit 9	I/O	4 mA	
A23	SA8	Address bit 8	I/O	4 mA	
A24	SA7	Address bit 7	I/O	4 mA	
A25	SA6	Address bit 6	I/O	4 mA	
A26	SA5	Address bit 5	I/O	4 mA	
A27	SA4	Address bit 4	I/O	4 mA	
A28	SA3	Address bit 3	I/O	4 mA	
A29	SA2	Address bit 2	I/O	4 mA	
A30	SA1	Address bit 1	I/O	4 mA	
A31	SA0	Address bit 0	I/O	4 mA	
A32	GND	Ground	N/A	N/A	

* PU = pull up; PD = pull down; S = resistance in series. All values in ohms.

Table 2–47. AT Expansion Bus Connector, B1-B32 (P1)

Pin	Signal Name	Function	In/Out	Current	PU/PD/S *
B1	GND	Ground	N/A	N/A	
B2	RESETDRV	System reset signal	OUT	4 mA	
B3	+5V	+5 Volt power	N/A	N/A	
B4	IRQ9	Interrupt request 9	IN	N/A	27K PU
B5	-5V	To J7-5	N/A	N/A	
B6	DRQ2	DMA request 2	IN	N/A	2.2K PD
B7	-12V	To J7-6	N/A	N/A	
B8	ENDXFR*	Zero wait state	IN	N/A	
B9	+12V	To J7-4	N/A	N/A	
B10	Key	Key pin	N/A	N/A	
B11	SMEMW*	Mem Write(lwr 1MB)	I/O	4 mA	22 S, 27K PU
B12	SMEMR*	Mem Read(lwr 1MB)	I/O	4 mA	22 S, 10K PU
B13	IOW	I/O Write	I/O	4 mA	22 S, 27K PU
B14	IOR	I/O Read	I/O	4 mA	22 S, 27K PU
B15	DACK3*	DMA Acknowledge 3	OUT	6 mA	
B16	DRQ3	DMA Request 3	IN	N/A	2.2K PD
B17	DACK1*	DMA Acknowledge 1	OUT	6 mA	
B18	DRQ1	DMA Request 1	IN	N/A	2.2K PD
B19	REFRESH*	Memory Refresh	I/O	4 mA	22 S,1K PU
B20	SYSCLK	Sys Clock	OUT	4 mA	
B21	IRQ7	Interrupt Request 7	IN	N/A	27K PU
B22	IRQ6	Interrupt Request 6	IN	N/A	27K PU
B23	IRQ5	Interrupt Request 5	IN	N/A	27K PU
B24	IRQ4	Interrupt Request 4	IN	N/A	10K PU
B25	IRQ3	Interrupt Request 3	IN	N/A	10K PU
B26	DACK2*	DMA Acknowledge 2	OUT	6 mA	
B27	TC	DMA Terminal Count	OUT	4 mA	
B28	BALE	Address latch enable	OUT	4 mA	
B29	+5V	+5V power	N/A	N/A	
B30	OSC	14.3 MHz clock	OUT	6 mA	33 S
B31	GND	Ground	N/A	N/A	
B32	GND	Ground	N/A	N/A	
* PU = pull up; PD = pull down; S = resistance in series. All values in ohms.					

Table 2–48. AT Expansion Bus Connector, C0-C19 (P2)

Pin	Signal Name	Function	In/Out	Current	PU/PD/S *
C0	GND	Ground	N/A	N/A	
C1	SBHE	Bus High Enable	I/O	4 mA	
C2	LA23	Address bit 23	I/O	12 mA	
C3	LA22	Address bit 22	I/O	12 mA	
C4	LA21	Address bit 21	I/O	12 mA	
C5	LA20	Address bit 20	I/O	12 mA	
C6	LA19	Address bit 19	I/O	12 mA	
C7	LA18	Address bit 18	I/O	12 mA	
C8	LA17	Address bit 17	I/O	12 mA	
C9	MEMR*	Memory Read	I/O	4 mA	27K PU
C10	MEMW*	Memory Write	I/O	4 mA	27K PU
C11	SD8	Data Bit 8	I/O	4 mA	4.7K PU
C12	SD9	Data Bit 9	I/O	4 mA	4.7K PU
C13	SD10	Data Bit 10	I/O	4 mA	4.7K PU
C14	SD11	Data Bit 11	I/O	4 mA	4.7K PU
C15	SD12	Data Bit 12	I/O	4 mA	4.7K PU
C16	SD13	Data Bit 13	I/O	4 mA	4.7K PU
C17	SD14	Data Bit 14	I/O	4 mA	4.7K PU
C18	SD15	Data Bit 15	I/O	4 mA	4.7K PU
C19	Key	Key Pin	N/A	N/A	
* PU = pull up; PD = pull down; S = resistance in series. All values in ohms.					

Table 2–49. AT Expansion Bus Connector, D0-D19 (P2)

Pin	Signal Name	Function	In/Out	Current	PU/PD/S *
D0	GND	Ground	N/A	N/A	
D1	MEMCS16*	16-bit Mem Access	IN	N/A	330 PU
D2	IOCS16*	16-bit I/O Access	IN	N/A	330 PU
D3	IRQ10	Interrupt Request 10	IN	N/A	27K PU
D4	IRQ11	Interrupt Request 11	IN	N/A	27K PU
D5	†		N/C	N/A	
D6	IRQ15	Interrupt Request 15	IN	N/A	27K PU
D7	IRQ14	Interrupt Request 14	IN	N/A	27K PU
D8	DACK0*	DMA Acknowledge 0	OUT	6mA	
D9	DRQ0	DMA Request 0	IN	N/A	2.2K PD
D10	DACK5*	DMA Acknowledge 5	OUT	6mA	
D11	DRQ5	DMA Request 5	IN	N/A	2.2K PD
D12	DACK6*	DMA Acknowledge 6	OUT	6mA	
D13	DRQ6	DMA Request 6	IN	N/A	2.2K PD
D14	DACK7*	DMA Acknowledge 7	OUT	6mA	
D15	DRQ7	DMA Request 7	IN	N/A	2.2K PD
D16	+5V	+5 Volt Power	N/A	N/A	
D17	MASTER*	Bus Master Assert	IN	N/A	330 PU
D18	GND	Ground	N/A	N/A	
D19	GND	Ground	N/A	N/A	

* PU = pull up; PD = pull down; SER = resistance in series. All values in ohms.

† IRQ12 is not available.

Interrupt and DMA Channel Usage

The AT bus provides several interrupt and DMA control signals. When the system is expanded with MiniModule products or plug-in cards that require either interrupt or DMA support, interrupt or DMA channels must be specifically selected. This typically involves setting switches or adding jumpers on the module. In most cases, these are not shared resources. It is important to configure the new module to use an interrupt or DMA channel not already in use. Table 2–50 and Table 2–51 provide a summary of the normal interrupt and DMA channel assignments on the Little Board/486*e* CPU.

Table 2–50. Interrupt Channel Assignments

Interrupt	Function
IRQ0*	ROM BIOS clock tick function, from Timer 0
IRQ1*	Keyboard interrupt
IRQ2*	Cascade input for IRQ8-15
IRQ3	Serial 2
IRQ4	Serial 1
IRQ5	Secondary Parallel port (option) / Serial 4 (option)
IRQ6	Floppy controller
IRQ7	Primary Parallel port (option) / Serial 3 (option)
IRQ8*	Reserved for battery-backed clock alarm
IRQ9**	Ethernet interface default**
IRQ10	Serial 4 (option)
IRQ11	Serial 3 (option)
IRQ12	Available
IRQ13*	Reserved for coprocessor *
IRQ14	IDE hard disk controller
IRQ15	Available

* Unavailable on the PC/104 bus.
** Corresponds to IRQ2 on PC's expansion bus.

Table 2–51. DMA Channel Assignments

Channel	Function
0	Available for 8-bit transfers
1	Available for 8-bit transfers (Multimode Parallel port)
2	Floppy controller
3	Available for 8-bit transfers
4	Cascade for channels 0-3
5	Available for 16-bit transfers
6	Available for 16-bit transfers
7	Available for 16-bit transfers

Table 2–52 summarizes the available interrupt assignments for all subsystems on the Little Board/486*e* CPU. Use the table to plan which interrupts to use in your system. Factory defaults are shown in gray.

Table 2–52. Summary of IRQ Options

	IRQ										
Function	3	4	5	6	7	9	10	11	12	14	15
Serial 1		✓									
Serial 2	✓										
Serial 3					✓			✓			
Serial 4			✓				✓				
Parallel			✓		✓						
Floppy				✓							
IDE										✓	
Ethernet	✓					✓	✓	✓			
Video	(None)										

SETUP Overview

This section describes the SETUP function. It describes each option that can be set using SETUP. Additional sections describe important options that can be set for each major functional block of the board.

Note

The SETUP descriptions in the following section also contain much useful information about each SETUP topic. Review these sections even if you already know how to set the SETUP parameters.

This section assumes users are familiar with DOS. It does not attempt to describe the standard DOS and ROM BIOS functions. Refer to the appropriate DOS and PC reference manuals for information about DOS, its drivers and utilities, and about the software interface of the onboard ROM-BIOS. Where Ampro has added to or modified standard functions, these will be described.

The Ampro Common Utilities manual contains detailed descriptions of the Ampro utility programs supplied on the Utility diskette that is included with the Little Board/486*e* Quick Start Kit or Development Platform Kit.

Many options provided on the Little Board/486*e* CPU are controlled by the SETUP function. Activating the SETUP function can access these options. The parameters are displayed on four screens. To configure the board, modify the fields on these screens and save the results in the onboard *configuration memory*. Configuration memory consists of portions of the CMOS RAM in the battery-backed real-time clock chip and an Ampro-unique configuration EEPROM. To enhance embedded-system reliability, the contents of the EEPROM mirror the contents of the CMOS memory. The EEPROM retains your configuration information even if the clock's backup battery should fail. If you choose to use the Little Board/486*e* CPU without a battery, the system takes its SETUP parameters from the EEPROM, providing battery-free operation.

The SETUP information is retrieved from configuration memory when the board is powered up or when it is rebooted with a CTL-ALT-DEL key pattern. Changes made to the SETUP parameters, with the exception of the real-time clock time and date settings do not take effect until the board is rebooted.

The SETUP function is located in the ROM BIOS. It can be accessed using CTRL-ALT-ESC while the computer is in the Power-On Self Test (POST), just before booting up. This is called *hot key* access. The screen displays a message indicating when you can enter CTRL-ALT-ESC. You can also enter the SETUP function from the DOS command line using the SETUP.COM program provided on the Ampro Common Utilities diskette.

Table 2–53 summarizes the choices found on each SETUP page.

Table 2–53. Functions on Each SETUP Page

Page	Menu Name	Functions
1	Standard (CMOS/EEPROM) Configuration	Set date and time Define floppy drives Define IDE hard disks Select video type Display DRAM quantity Set error halt conditions Enable/disable video shadow RAM Set POST display option
2	Options/Peripheral Configuration	Enable/disable extended BIOS functions Enable/disable serial ports Enable/disable parallel port Enable/disable floppy interface Enable/disable IDE interface Enable/disable hot key access to SETUP Set video display state Select POST display option Configure byte-wide socket Enable/disable serial boot loader Enable/disable watchdog timer Configure video display
3	Extended Serial Console Configuration	Configure serial port parameters for serial console output Configure serial port output handshake option Configure serial port parameters for serial console input Delete/include console port from DOS COM table
* SETUP pages 3 and 4 are available when you enable Extended BIOS from SETUP		

Note

Some SETUP options can put systems into an unrecoverable state; a display option can be set preventing the SETUP screens from being seen. Installing a jumper between J11-7 and J11-8 (Serial 1 DTR and RI) temporarily sets all SETUP functions to their default state, bypassing the SETUP parameters stored in the configuration memory so that SETUP can be reentered and the problem corrected.

SETUP Page 1—Standard (CMOS/EEPROM) Setup

The first SETUP page contains the parameters normally saved in CMOS RAM plus some additional parameters unique to the Little Board/486*e* CPU. The only parameters not auto saved in the EEPROM memory are the real-time clock date and time. If no battery is used or if the battery fails, the date and time will not be accurate. All other parameters are saved in the EEPROM.

Figure 2–13 shows what can be configured using SETUP page 1. Sections following the figure describe each option.

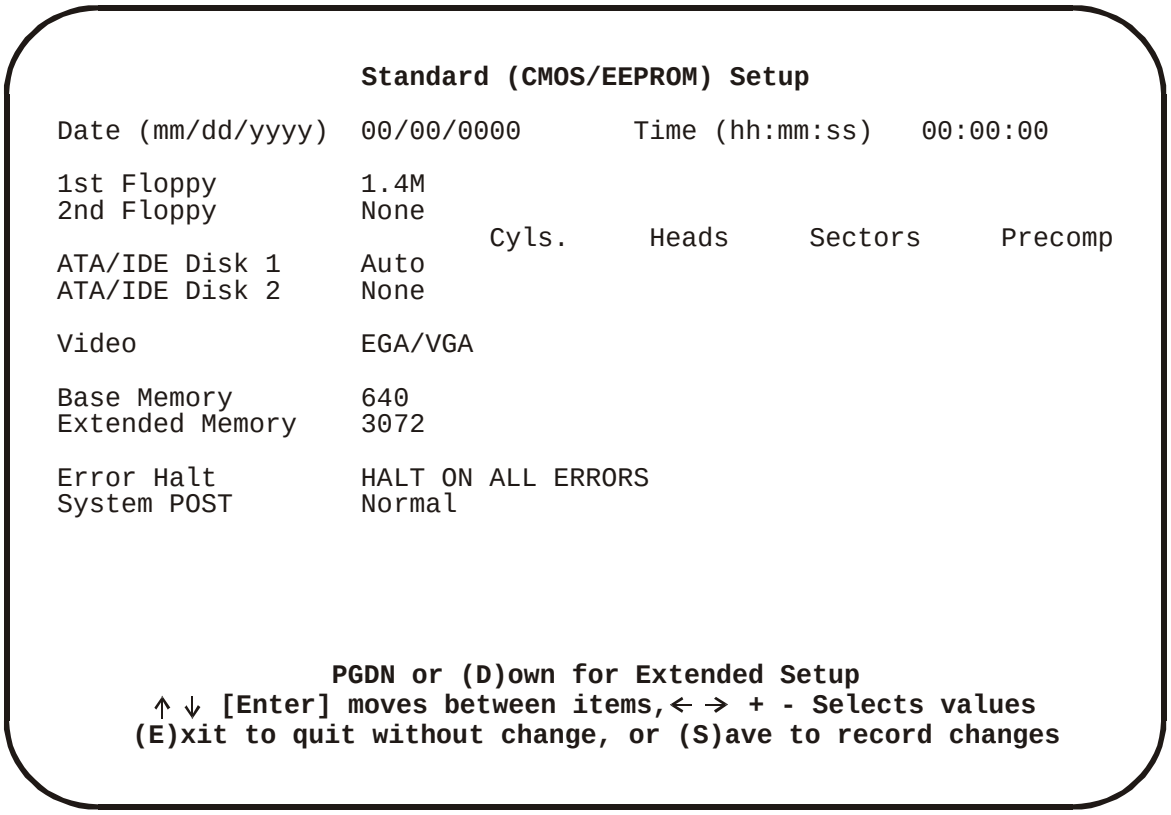


Figure 2–13. SETUP Page 1

Date and Time

The time shown on the first SETUP screen is continuously updated and reflects the current state of the hardware real-time clock. The new time and date entered is immediately written to the device. Enter the date in the form *mm/dd/yyyy*. The year requires all 4 digits. Enter the time in 24-hour format, in the form *hh:mm:ss*.

The ROM BIOS maintains the *system* real-time clock. It is incremented approximately 18.2 times per second by an interrupt from timer/counter 0. The ROM BIOS automatically initializes the *system* real-time clock from the *hardware* real-time clock upon system reset or power up. The accuracy of the hardware real-time clock depends on connecting a battery to the appropriate terminals on J5, the Utility connector. If a battery is not attached, the system time information does not remain accurate after a power cycle.

Floppy Drives

The ROM BIOS supports all of the popular DOS-compatible floppy disk formats. This includes all the 5-1/4 inch and 3-1/2 inch floppy formats—360K, 720K, 1.2M, and 1.44M byte. The ROM BIOS also supports dual-capacity use of high density floppy drives, systems can be read and booted from 360K floppies in a 1.2M 5-1/4 inch drive, and from 720K floppies in a 1.44M 3-1/2 inch drive.

Drive Parameter Setup

Enter the number and type of floppy drives in the system. If the drives connected to the system do not match the parameters in the configuration memory, POST displays an error message. To eliminate the error message, set the drive parameters to match your floppy drives.

IDE Hard Disk Drives

The ROM BIOS supports one or two hard disk drives connected to the IDE interface. The IDE SETUP parameters are used for setting the physical parameters of the drives you install in your system. Physical drives can have one or more logical partitions. Up to eight *logical* drives or drive partitions can be installed but only two physical drives can be used. Older versions of DOS may limit the number of logical drives that can be installed.

No parameters are displayed for Auto detect hard disk. All IDE/ATA drives should be configured for Auto. Manual entries are for legacy use only to support Western Digital and similar MFM AT bus controllers.

To configure the system for one or two IDE drives, set the drive parameters with SETUP, as outlined here:

- **Drive Types**—The configuration memory contains a default list of parameters that specify the physical format of each drive. Each *type* specifies the total number of cylinders, number of heads, cylinder to begin pre-compensation, landing zone cylinder number, and the number of sectors per cylinder. The drive manufacturer supplies these parameters. The list contains legacy values, standard for PCs—a number of older (smaller) drives are defined.
  1. Two special drive types, 48 and 49, let you enter drive parameters manually. If no built-in drive type matches your drive, select drive type 48 or 49 and enter the drive parameters in the fields provided.
  2. Drive type **AUTO** selects **Autoconfigure**. Autoconfigure queries the drive for its parameters. All IDE/ATA drives respond to the query, allowing the BIOS to set the drive parameter values automatically. This option also provides Logical Block Addressing (LBA) capability, which supports drives larger than 512M bytes.

Note

LBA uses a translation scheme to convert physical heads, sectors and cylinders to logical block numbers. Due to differences in the translation schemes used by different system BIOSes, LBA-compatible drives that were formatted on Ampro systems may not function properly in other systems that support LBA mode. However, due to the intelligent translation algorithm in the Ampro BIOS, drives formatted in other systems may be usable on the Little Board/486*e* CPU.

- **Drive Selection**—Besides specifying the physical characteristics of each IDE drive, how they are to be used by the ROM BIOS must also be specified. Two factors control how they are used, drive number jumper(s) and the DOS disk map.
  1. An IDE drive can be jumpered as a **master** or **slave**. Each manufacturer's drive is different. Refer to the drive's technical documentation to find out how to jumper the drives. Drives default to **master** from the factory. If a system has only one IDE drive, it is generally already set up properly.
  2. Use the SETUP Extended Hard Disk Configuration menu (SETUP page 3) to enter the IDE drive(s) in the DOS disk map. Disk 1 in the map is logged by DOS as drive C, Disk 2 as drive D, and so on. See the description of SETUP page 3 for details.

Once the system's configuration memory is set, the IDE drive(s) can be formatted and otherwise prepared normally. Refer to the O/S and disk drive documentation for specific procedures and requirements.

Video

Specify the initial video mode by selecting one of the following:

- **Mono**
- **Color40**
- **Color80**
- **EGA/VGA**

If the video display card is VGA, super VGA, or any other high-resolution standard, specify **EGA/VGA** regardless of how it is configured to initialize.

DRAM Memory

The ROM BIOS automatically sets the amount of memory it discovers during Power-On Self-Test (POST) and stores the result when you save the configuration values when exiting SETUP. If the amount of memory installed on the board is changed however, SETUP must be run and a save performed before exiting. This updates the configuration memory to reflect the new memory size. Until this procedure is accomplished, an error message appears during POST.

If an error message appears during POST and the amount of memory installed was not changed, it indicates that at least part of the memory is not functioning properly.

Error Halt

Select which kinds of errors will halt the POST. If the module is used without a keyboard, set this option to *not* halt on keyboard error.

System POST

At boot time, the BIOS runs a series of tests called the Power-On Self Test or POST. Options in the Ampro BIOS allow the POST to be customized in order to control how fast the computer powers up. It also controls what the user sees at power up time. The choices are:

- **Normal**—Displays the results of all tests
- **Fast**—Faster than Normal POST because it uses a shorter memory test
- **Express**—Skips most tests and does not display POST test results on the screen

SETUP Page 2—Options/Peripheral Configuration

Use SETUP page 2 to enable or disable many of the functions and peripherals provided on the Little Board/486*e* CPU. Figure 2–14 shows what can be configured on SETUP page 2, and the sections that follow describe each parameter.

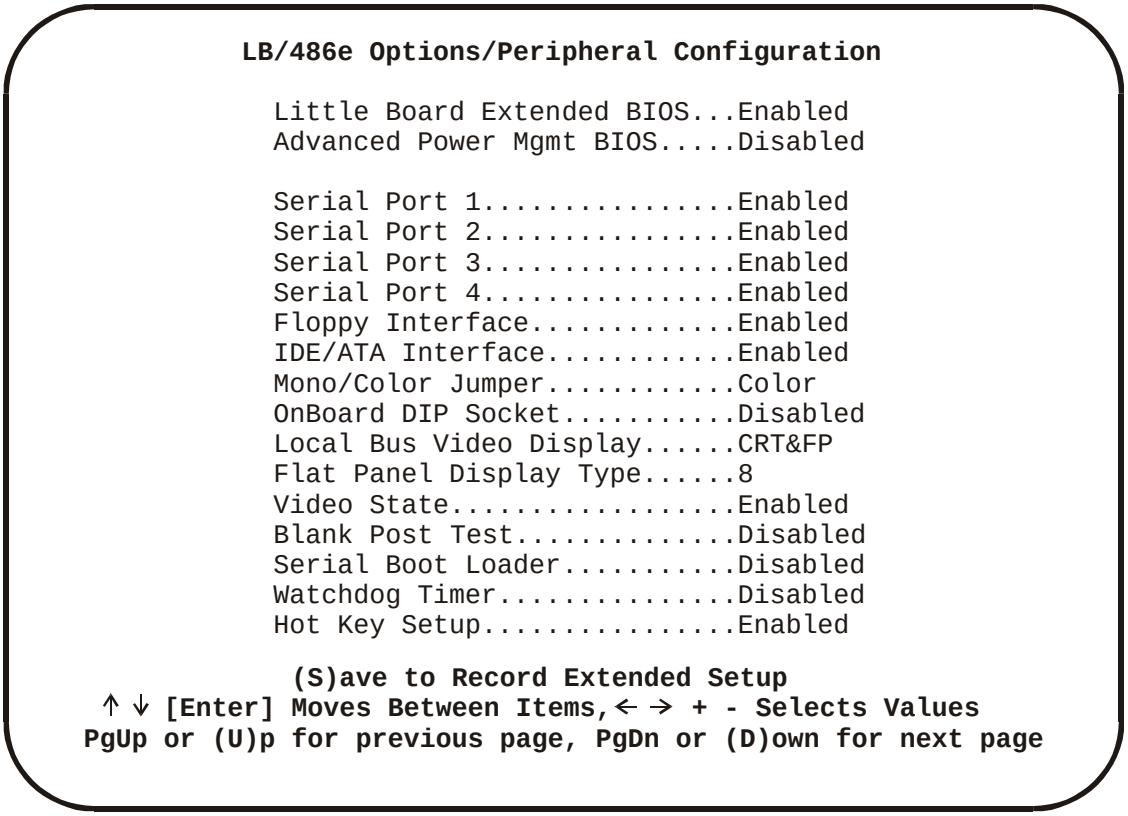


Figure 2–14. SETUP Page 2

Extended BIOS

The Ampro Extended BIOS is normally enabled allowing access to SETUP pages three and four and the features they define. If the BIOS extensions are not used they can be disabled with this parameter. Some UNIX implementations or other operating systems may require disabling the extended portion of the BIOS. Application Notes and other documentation describing the specific Ampro extended BIOS services and how they are used are available from Ampro Technical Support.

Serial Port

Use SETUP to independently enable or disable either of the two onboard serial ports. When SETUP is used to enable or disable a port, the change does not take effect until the system is rebooted.

The I/O addresses and interrupt assignments (IRQs) for the serial ports cannot be changed. Table 2–54 lists the I/O addresses and IRQs of each port. These resources are freed for use by other peripherals installed on the PC/104 bus when their respective ports are disabled.

Table 2–54. Serial Port Resources

Port	Address
Serial 1	3F8h – 3FFh
Serial 2	2F8h – 2FFh
Serial 3	3E8h – 3EFh
Serial 4	2E8h – 2EFh

The BIOS normally logs Serial 1 and Serial 2 as COM1 and COM2. COM1 and COM2 are logical designations, not physical values. When the system boots, the BIOS scans the standard serial port addresses and installs the first port it finds as COM1. If it finds a second port, it installs that one as COM2, and so on. If you disable a serial port, the designations of all higher-numbered COM ports changes. See the Serial Port section of this Chapter for more information.

Parallel Port

The Little Board/486*e* parallel port SETUP allows it to be enabled as the primary or secondary port. The I/O ports and interrupt request channels are freed for use by other peripherals installed on the PC/104 bus when the parallel port is disabled. Table 2–55 summarizes the resources that can be used for the parallel port.

Table 2–55. Parallel Port Resources

Selection	I/O Address	Interrupt
Primary	0378h - 037Fh	IRQ7
Secondary	0278h - 027Fh	IRQ5
Disable	None	None

The BIOS normally logs the primary and secondary parallel ports as LPT1 and LPT2. LPT1 and LPT2 are logical designations, not physical values. When the system boots, the BIOS scans the standard parallel port addresses and installs the first port it finds as LPT1. If it finds a second port, it installs that one as LPT2, and so on. If a parallel port is disabled, the designation of all higher-numbered LPT ports change.

For further information about utilizing the parallel port, see the section on the bi-directional Parallel Port.

Floppy Interface Enable

Enable or disable the onboard floppy interface. When disabled, the I/O ports assigned to the floppy controller become available, allowing them to be used by other devices installed on the expansion bus. Table 2–56 lists the resources used by the floppy controller.

Table 2–56. Floppy Controller Resources

Selection	I/O Address	IRQ	DMA
Enabled	03F2h - Digital Output Register 03F4h - Main Status Register 03F5h - Data Register 03F7h - Control Register	IRQ6	DMA 2
Disable	None	None	None

IDE Interface Enable

Enable or disable the onboard IDE hard disk interface. When disabled, the I/O ports and IRQ assigned to the IDE controller become available, allowing them to be used by other devices installed on the expansion bus. Table 2–57 lists the resources used by the IDE interface.

Table 2–57. IDE Controller Resources

Selection	I/O Address	Interrupt
Enabled	01F0h - 01F7 Control and Data Registers 03F7h Shared with FDC	IRQ14
Disable	None	None

If an IDE drive is attached to J6, disabling the IDE interface does not free the IRQ14 interrupt since it is connected directly to the drive. The cable must be disconnected.

Hot Key Setup Enable

In some embedded systems, end-users are not permitted to use the *hot-key* sequence (CTRL-ALT-ESC) to enter SETUP. Hot key access to SETUP can be enabled or disabled using this parameter. This also prevents “+++” from entering SETUP when using the serial console feature.

Video State

Video State can be set to Enabled or Inhibited. Inhibited ***blanks*** the display until an application program makes a call to the Video Restore State function in the video BIOS through INT10h. This provides a means of controlling what appears on the screen when the system starts up. This option can be used to inhibit the POST test display and everything else that DOS or an application would display, until a call is made to the video BIOS.

The following is an example of code that reenables the display inhibited by this option:

```
;=====================================================================
init: mov ah,1ch
      mov al,-1
      mov bx,414Dh
      mov cx,5052h
      int 10h
;=====================================================================
```

Blank Post Test

The blank post test either enables or disables the POST display. If set to **Disabled**, the messages from the POST is not be sent to the console. Video display is restored when POST is completed. To inhibit display of a broader range of system and application messages, see Video State, above.

Byte-Wide Socket Configuration

The byte-wide socket, S0 can be configured for its *starting address* and the *size* of the memory block in which it appears to the processor, or it can be disabled. Whether or not the socket should be enabled during the boot process can also be specified.

Table 2–58 lists the socket address configuration options that are available.

Table 2–58. Byte-Wide Socket Configuration

Size	Address
Disabled	None
64K bytes	D0000h – DFFFFh
64K bytes	E0000h – EFFFFh
128K bytes	D0000h – EFFFFh

Ampro provides several extended BIOS function calls that allow software control of the byte wide socket state such as:

- Enable/disable
- Programming control for flash EPROMs

Contact Ampro Technical Support for additional information regarding these services.

Hardware jumpers can also be set to configure the byte-wide socket for any device installed in S0. Jumper positions are provided earlier in this chapter.

The byte wide socket has no hardware provisions for paging large memory devices, and is not recommended for SSD (64K byte maximum).

Serial Boot Loader Enable

This parameter enables or disables the Serial Boot Loader option in the Ampro ROM BIOS. The serial boot loader allows booting from either of the onboard serial ports much in the same way you would boot from a local hard disk or from a LAN. A description of the Serial Boot Loader is provided in the Ampro Common Utilities manual (see SERLOAD and SERPROG). If the Serial Boot Loader is used, set this parameter to *Enabled*.

Watchdog Timer Configuration

This parameter allows the time duration of the watchdog timer to be set for monitoring the boot process. It can be set to 30, 60, or 90 seconds, or it can be disabled. A description of the related WATCHDOG utility program can be found in the Ampro Common Utilities manual.

Local Bus Video Display

If you will be using a CRT display, select CRT. If you will be using a flat panel display, select FP. If you will be using both types of display, select FP&CRT. If you select FP or FP&CRT, select a flat panel display type (see below).

Flat Panel Display Type

There are up to 8 pre-installed flat panel video BIOS configurations available from SETUP, numbered 1 through 8. Select the panel you want by selecting its number. A list of supported panels is provided on the Utilities diskette.

Installing a Modified BIOS to Support a New Panel

If you wish to use an unsupported panel for your application, you must modify the video BIOS to support the new panel. Ampro provides a video BIOS modification kit to do this. Contact your Ampro sales representative or Ampro Technical Support for information about the Little Board/486*e* Flat Panel BIOS Modification Kit.

Once you have modified the video BIOS to support your new panel, you must install it on the Little Board/486*e* CPU. Follow the instructions in “Developing a Custom BIOS for an Unsupported Flat Panel,” earlier in this chapter.

SETUP Page 3—Serial Console Configuration

The ROM BIOS includes a unique set of features that allow full access to the system at any time over standard RS-232 serial ports. An embedded system can take advantage of these remote access capabilities using the serial console functions in the following ways:

- **Serial console**—Use Serial 1 or Serial 2 as a console. Use a serial terminal to replace the standard video monitor and keyboard.
- **Serial boot loader**—Boot from a serial port in much the same manner as booting from a local hard disk or from a network. This feature is enabled or disabled with the **Serial Boot Loader** option on Page 2 of SETUP.
- **Serial programming**—Automatically update system software, through a serial port. This feature permits replacing code in a FLASH device installed in the byte-wide socket.

For more information about these serial console functions, see *Serial Console Features*, under *Serial Ports*.

Figure 2–15 shows the options you can set for the serial console. Since DOS normally initializes the serial ports during boot, you have the option to remove the serial console port from DOS's COM port table. By doing this, the values you set on SETUP screen 4 remain after you boot DOS.

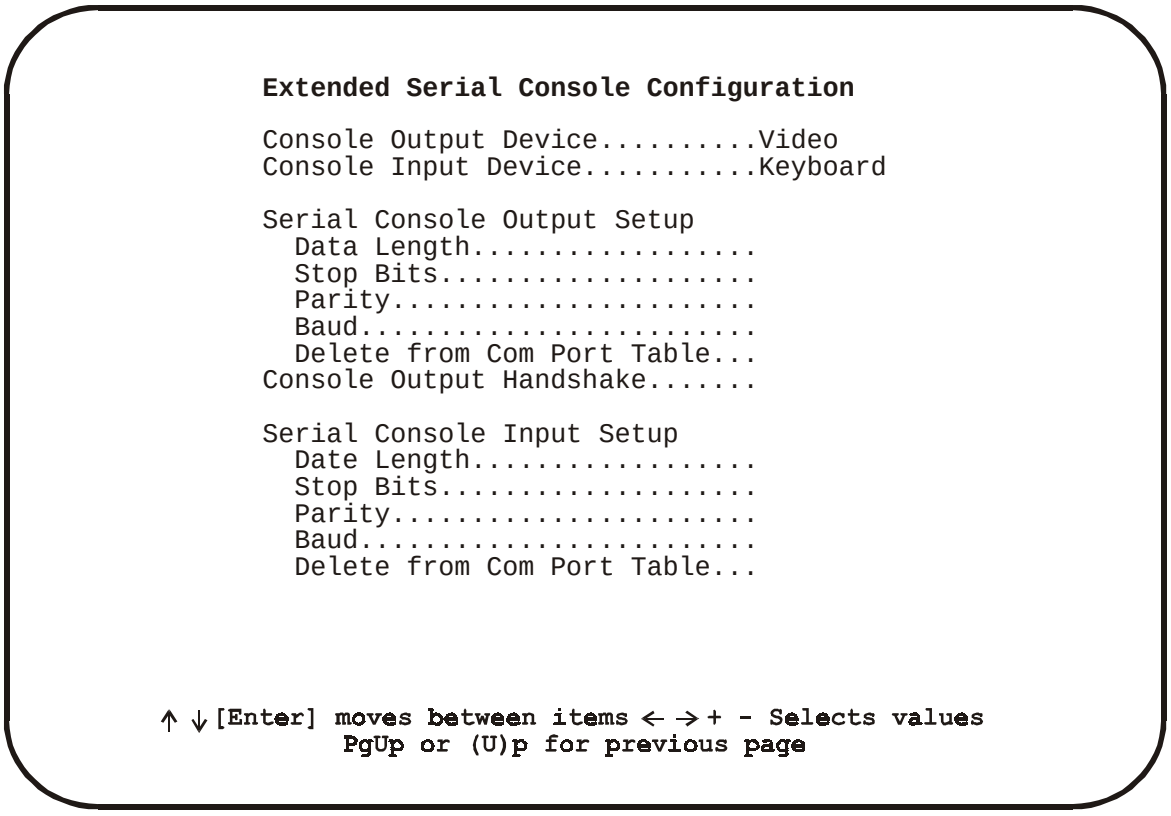


Figure 2–15. SETUP Page 3

This section describes the SETUP parameters found on the Extended Serial Console Configuration screen.

- **Console Output Device**—Select the console output device, either Video, Serial 1, Serial 2, or None.
- **Console Input Device**—Select the console input device, either the PC Keyboard, Serial 1, Serial 2, or None.
- **Serial Console Output Setup**—Enter the communication parameters for your console output serial port. Set the data length, stop bits, parity, and baud rate to match the serial output device.
- **Console Output Handshake**—Enable or disable hardware handshaking. If enabled, the DSR and CTS signals control the data flow. Be sure to connect the DSR and CTS signals on the serial port's connector to the appropriate handshake signals on the external serial device's interface connector.
- **Serial Console Input Setup**—Enter the communication parameters for the console *input* serial port. Set the data length, stop bits, parity, and baud rate to match the serial input device.
- **Delete from COM Port Table**—When DOS boots, it initializes the system serial ports. Different versions of DOS may set the ports to different default settings. Enabling this option causes the BIOS not to include console serial device(s) in the COM port table. This prevents DOS from changing the assigned port values entered in the SETUP screen.

Caution

Be careful when changing the console configuration. If *None* is specified for console input and output, there is no console access to the system. This state can be recovered by removing the serial console plug from the primary serial port connector and shorting pins J11-7/8.

The SETUP.COM Program

The SETUP.COM utility can be used from the command line to access the same SETUP functions as the *hot key* code, CTRL-ALT-ESC. SETUP.COM also adds additional functionality, such as the ability to load and store configuration settings to a disk file. This same feature is used to store OEM information in the configuration memory EEPROM. SETUP.COM is on the Ampro Common Utilities diskette, included with the Little Board/486*e* Development Kit. See the Ampro Common Utilities manual for more information regarding SETUP.COM usage.

Creating Configuration Files with SETUP.COM

The Ampro SETUP utility, SETUP.COM, offers the following options for command line entry:

```
SETUP [-switches]  [ @file.ext  |  Wfile.ext ]
```

The supported switches and their meaning are shown in Table 2–59.

Table 2–59. SETUP.COM Command Switches

Switch	Function
?	Display a usage help screen
T	Set the (hardware) real-time clock time and date from the current DOS time and date.
@*file.ext*	Writes the specified file to the board's CMOS RAM and configuration EEPROM. Drive and path are optional in the file name.
W*file.ext*	Write CMOS RAM and EEPROM contents to the file specified. The file name may contain an optional drive and path.

You can save a copy of the current contents of the board's configuration memory to a disk file by using the W switch. The data saved includes the entire contents of the nonvolatile configuration EEPROM. The first 512 bits are the SETUP information (excluding time and date), the next 512 bits are available for OEM storage. See Ampro Application Note AAN-8805 for a description of how to use the OEM storage portion of the EEPROM.

The file you create with this menu option can be used as a source for programming the configuration memory of a Little Board/486*e* CPU at a later time.

As an example, the following command initializes the EEPROM values with a previously saved configuration:

```
C>SETUP  @SYSTEM.A
```

Assuming you created the file SYSTEM.A with SETUP's write option, SETUP will initialize the EEPROM configuration memory using the contents of SYSTEM.A.

Using SETUP with the write and read parameters can be useful when many boards must be initialized automatically, or when you want to change between several predefined system configurations.

Operation with DOS

The Little Board/486*e* CPU supports IBM's PC-DOS or Microsoft's MS-DOS, Version 3.3 or later, or any version of Digital Research's DR DOS as the disk operating system. Any differences between these similar operating systems are noted in the text where applicable.

Caution

Sometimes MS-DOS is customized by a manufacturer for a specific system and may not work on the Little Board/486*e* CPU. Use DR DOS (supplied by Ampro), IBM PC-DOS (supplied by IBM), or the generic version of MS-DOS (supplied by Microsoft on an OEM basis).

EMS Option—The Little Board/486*e* CPU can emulate the Lotus-Intel-Microsoft Expanded Memory Specification Version 4.0 (LIM EMS 4.0), with the memory management capability of the 80486DX2/4 CPU, under control of a device driver. Such drivers are available with the newer versions of DOS. With Microsoft MS-DOS, the driver is called EMM386.EXE.

Serial Ports—DOS normally supports the board's four serial ports as COM1, COM2, COM3, and COM4.

At boot time, DOS initializes the serial ports, assigning them their COM port designations and their communication parameter settings. Although this might vary with different types and versions of DOS, typical communication parameter settings are 2400 baud, even parity, 7 bits, and 1 stop bit.

Usually an application program that uses a serial port will access the port's hardware and reinitialize the communication parameters to other values, based on settings that the user has entered when configuring the application program.

Parallel Port—The Parallel Printer port is normally the DOS LPT1 device. Most application software uses LPT1 as the default printer port. If you enable the port, printing to it is automatic.

The following DOS commands can be used to test printing with the parallel printer:

`A>COPY CONFIG.SYS LPT1`	Prints contents of CONFIG.SYS
`A>DIR >LPT1`	Prints the directory

In addition, the <PrtSc> (Print Screen) key will print the contents of the video screen to the LPT1 device. Also, you can use the Printer Echo function to print all characters typed on the keyboard. The command <Ctrl-P> enables the Printer Echo function. Entering <Ctrl-P> again disables Printer Echo.

Disk Drives—Older versions of DOS require you to divide disk drives larger than 32M bytes into more than one partition. More recent versions permit drives to be up to 2G bytes, though IDE drives are BIOS limited to 512M bytes. Larger IDE drives typically provide a driver to get around the BIOS limit.

Utility Software Overview

The Little Board/486*e* Development Kit provides a number of software utilities on the Ampro Common Utilities diskette. Some of the programs provided on this diskette are:

FLASHWRI—Flash PROM utility for writing program images to Flash devices in byte-wide sockets.

SETUP—A utility used to access the ROM BIOS SETUP function from the DOS command line.

SERLOAD—A serial loader utility for downloading files from a remote host prior to system boot.

SERPROG—A utility to program Flash byte-wide devices from a serial port.

TVTERM—A Televideo 900-series terminal emulator.

WATCHDOG—Used to stop, start, or retrigger the watchdog timer function.

These utilities and others are described in the Ampro Common Utilities manual.

Chapter 3

Technical Specifications

Little Board™/486*e* CPU Specifications

The following section provides technical specifications for the Little Board™/486*e* CPU.

CPU/Motherboard

- CPU: 3.3 V 100 MHz or 133 MHz 80486
- System RAM:
  - Socket for 168-pin DIMM, FPM or EDO only
  - Supports up to 64M bytes total RAM
- 15 interrupt channels (8237-equivalent)
- 7 DMA channels (8259-equivalent)
- 3 programmable counter/timers (8253-equivalent)
- Standard PC/AT keyboard port
- Standard PC speaker port with .1 watt output drive
- Battery-backed real-time clock and CMOS RAM
  - Up to 10 year battery life
  - Supports battery-free operation
- Award ROM BIOS with Ampro embedded-system extensions

Embedded-PC System Enhancements

- One 32-pin byte-wide memory socket:
  - Usable with 128K to 1M byte EPROMs, 128K to 512K byte FLASH EPROMs, 128K to 512K byte SRAMs, or 128K to 512K byte NOVRAMs (Non-volatile RAMs)
  - Onboard programming of 5 V FLASH EPROMs
  - Configurable as 64K or 128K byte window, addressed in the range of D0000h to EFFFFh
  - Supported by Ampro SSD Support Software and many third-party operating systems
- 2K-bit configuration EEPROM:
  - Stores system SETUP parameters
  - Supports battery-free boot capability
  - 512 bits are available for OEM use
- Watchdog Timer:
  - Utilizes the onboard real-time clock alarm function
  - Timeout triggers a hardware reset or non-maskable interrupt
- Powerfail NMI triggers when +5 Volt power drops below +4.65 Volts.

Onboard Peripherals

This section describes standard peripherals found on every Little Board/486*e* CPU.

- Four buffered serial ports with full handshaking:
  - Implemented with 16550-equivalent controllers with built-in 16-byte FIFO buffers
  - Onboard generation of ±9 Volts for RS-232C signal levels
  - Channel two supports either RS-232C (direct connection) or RS-485 Adapter
  - Logged as COM1, COM2, COM3, and COM4 by DOS.
- PC-compatible Parallel Port:
  - Superset of standard LPT printer port.
  - Bi-directional data lines
- Floppy Disk Controller:
  - Supports one or two drives
  - Reliable digital phase-locked loop circuit
  - Supports all standard PC/AT formats: 360K, 1.2M, 720K, 1.44M
- IDE Disk Controller:
  - Standard PC-compatible IDE hard disk controller
  - Supports up to two hard disk drives
- PCI Flat Panel/CRT Video Controller
  - Supports CRT, LCD, and EL displays
  - Uses the C&T 65550 High Performance Flat Panel/CRT VGA Controller
  - Onboard display RAM 2M bytes standard
  - Video modes and resolutions, see Table 3–1 and 3–2
  - Supports interlaced or non-interlaced displays in up to 1280 x 1024 resolution modes
  - Supports 24-bit True Color at 800 x 600 VGA resolution
  - GUI accelerator for enhanced performance
  - Video BIOS supports VESA super VGA modes
  - Software programmable flat panel interface. Flat panel video BIOS contained in an onboard Flash EPROM device for easy customization
  - Optional LCD Bias Supply. Circuit board plugs on to connector on the Little Board/486*e* CPU
    - Supplies 15 V < Vee < 30 V DC, positive or negative polarity, at 30 mA (max)
    - Voltage level (LCD contrast control) adjustable with an onboard or external potentiometer
    - Sequences LCD power supplies to protect display
    - Implements advanced power management functions

Table 3–1. Supported CRT Video Modes—Standard VGA

Mode	Display Mode	Colors	Text	Font	Pixels	Clock (MHz)	Horiz (KHz)	Vert (Hz)
0+, 1+	Text	16	40x25 40x25 40x25	9x16 8x14 8x8	360x400 320x350 320x200	28.322 25.175 25.175	31.5	70
2+, 3+	Text	16	80x25 80x25 80x25	9x16 8x14 8x8	720x400 640x350 640x200	28.322 25.175 25.175	31.5	70
4	Graphics	4	40x25	8x8	320x200	25.175	31.5	70
5	Graphics	4	40x25	8x8	320x200	25.175	31.5	70
6	Graphics	2	80x25	8x8	640x200	25.175	31.5	70
7+	Text	Mono	80x25 80x25 80x25	9x16 9x14 9x8	720x400 720x350 720x350	28.322	31.5	70
D	Planar	16	40x25	8x8	320x200	25.175	31.5	70
E	Planar	16	80x25	8x8	640x200	25.175	31.5	70
F	Planar	Mono	80x25	8x14	640x350	25.175	31.5	70
10	Planar	16	80x25	8x14	640x350	25.175	31.5	70
11	Planar	2	80x30	8x16	640x480	25.175	31.5	60
12	Planar	16	80x30	8x16	640x480	25.175	31.5	60
13	Packed Pixel	256	40x25	8x8	320x200	25.175	31.5	70

CRT Support for Standard Video Modes

- PS/2 fixed frequency analog CRT monitor or equivalent. 31.5/35.5 KHz horizontal frequency.
- Multi-frequency CRT monitor. 37.5 KHz minimum horizontal frequency.
- Multi-frequency high-performance CRT monitor. 48.5 KHz minimum horizontal frequency.

Table 3–2. Supported CRT Video Modes—Extended Resolution

Mode	Display Mode	Colors	VESA Mode	Font	Pixels	Clock (MHz)	Horiz (KHz)	Vert (Hz)	Mem.
20	Pack Pixel	16	120	8x16	640x480	25.175 31.5 36	31.5 37.5 43.3	60 75 85	256K 256K 256K
22	Pack Pixel	16	122	8x16	800x600	36 40 49.5 56025	35.1 37.9 46.9 53.7	56 60 75 85	256K 256K 256K 256K
24	Pack Pixel	16	124	8x16	1024x768	65 78.75 94.5	48.5 60 68.7	60 75 85	512K 512K 512K
24I	Pack Pixel	16	124	8X16	1024X768	44.900	35.5	43	512K
28	Pack Pixel	16	128	8x16	1280 x 1024	78.75 108	47 64	43 60	1024K 1024K
2A*	-	16	-	8x16	1600 x 1200	-	-	-	938
30	Pack Pixel	256	101	8x16	640x480	25.175 31.5 36	31.5 37.5 43.3	60 75 85	512K 512K 512K
31	Pack Pixel	256	100	8x16	640x400	25.175	31.5	70	256K
32	Pack Pixel	256	103	8x16	800x600	36 40 49.5 56.25	35.1 37.9 46.9 53.7	56 60 75 85	512K 512K 512K 512K
34	Pack Pixel	256	105	8x16	1024x768	44.9 65 78.75 94.5	35.5 48.4 60 68.7	43(I) 60 75 85	1024K 1024K 1024K 1024K
38	Pack Pixel	256	107	8x16	1280 x 1024	78.75 108	47 64	43 60	1280K 1280K
3A*	-	256	-	8x16	1600 x 1200	-	-	-	1875K
40	Pack Pixel	32K	110	8x16	640x480	25.175 31.5 36	31.5 37.5 43.3	60 75 85	1024K 1024K 1024K
41	Pack Pixel	64K	111	8x16	640x480	25.175 31.5 36	31.5 37.5 43.3	60 75 85	1024K 1024K 1024K
42	Pack Pixel	32K	113	8x16	800x600	36 40 49.5 56.25	35.1 37.9 46.9 53.7	56 60 75 85	1024K 1024K 1024K 1024K
(The “I” in the Mode # column indicates “Interlaced.”) (* Modes 2AH and 3AH are for flat panel only.)									

Table 3–2. Supported CRT Video Modes—Extended Resolution (cont.)

Mode	Display Mode	Colors	VESA Mode	Font	Pixels	Clock (MHz)	Horiz (KHz)	Vert (Hz)	Mem.
43	Pack Pixel	64K	114	8x16	800x600	36 40 49.5 56.25	35.1 37.9 46.9 53.7	56 60 75 85	1024K 1024K 1024K 1024K
44	Pack Pixel	32K	116	8x16	1024 x 768	44.9 65	35.5 48.4	43(I) 60	1536K 1536K
45	Pack Pixel	64K	117	8x16	1024 x 768	44.9 65	35.5 48.4	43(I) 60	1536K 1536K
50	Pack Pixel	16M	112	8x16	640x480	25.175 31.5 36	31.5 37.5 43.3	60 75 85	1024K 1024K 1024K
52	Pack Pixel	16m	115	8x16	800x600	36 40	35.1 37.9	56 60	1536K 1536K
6A	Planar	16	102	8x16	800x600	36 40 49.5 56.25	35.1 37.8 46.9 53.7	56 60 75 85	256K 256K 256K 256K
64	Planar	16	104	8x16	1024 x 768	44.9 65 78.75 94.5	35.5 48.4 60 68.7	43(I) 60 75 85	512K 512K 512K 512K
68	Planar	16	106	8x16	1280 x 1024	78.75 108	47 64	43 60	768K 768K
70	Pack Pixel	256	101	8x16	640x480	25.175 31.5 36	31.5 37.5 43.3	60 75 85	512K 512K 512K
71	Pack Pixel	256	100	8x16	640x400	25.175	31.5	70	256K
72	Pack Pixel	256	103	8x16	800x600	36 40 49.5 56.25	35.1 37.9 46.9 53.7	56 60 75 85	512K 512K 512K 512K
74	Pack Pixel	256	105	8x16	1024x768	44.9 65 78.75 94.5	35.5 48.4 60 68.7	43(I) 60 75 85	1024K 1024K 1024K 1024K
78	Pack Pixel	256	107	8x16	1280 x 1024	78.75 108	47 64	43 60	1280K 1280K
(The “I” in the **Mode #** column indicates “Interlaced.”) (* Modes 2AH and 3AH are for flat panel only.)									

- Ethernet LAN Interface:
  - Complies with IEEE 802.3 (ANSI 8802-3)
  - Controller: SMC9000-series
  - Topology: Ethernet bus, using CSMA/CD
  - Media interface options: 10BaseT (twisted pair), through an onboard RJ45 connector
  - Data rate: 10M bits per second
  - Data buffer: 4608 byte RAM, accessed through I/O ports
  - I/O base address options: software selectable
  - Interrupt options: IRQ3, IRQ9 (default), IRQ10, IRQ11
  - DMA: not used
  - Boot ROM image can be installed in the board's byte-wide socket, only in S0

Support Software

- Enhanced Embedded-PC BIOS features:
  - Solid State Disk (SSD) support
  - Watchdog timer (WDT) support
  - Fast boot and blank POST options
  - Fail-safe boot logic
  - Battery-free boot
  - Serial console option
  - Serial loader option
  - EEPROM access function
  - Advanced Power Management (APM) support
  - BIOS OEM customization hooks

  See the Ampro Embedded-PC BIOS data sheet for additional details about these features.

- Software Utilities includes:
  - SETUP utility
  - Watchdog timer support
  - Power management support
  - Serial access and development support
  - Display controller support
  - Ethernet controller support

Mechanical and Environmental Specifications

- Dimensions: 8.0 x 5.75 x 1.2 inches (146 x 203 x 30 mm.). Refer to Figure 3–1 for mounting dimensions.
- Provision for system expansion with one or more Ampro MiniModule products or other PC/104 expansion modules.
- Power requirements (typical, with 16M byte DRAM):

  100 MHz 80486DX4 CPU: 1.46 Amps at +5V ±5%
- Operating environment:

  Standard: 0° to 70° C (with adequate airflow)

  Extended temperature range can be tested by special order. Contact Ampro for details.

  5 to 95% relative humidity (non-condensing)
- Storage temperature: -55° to +85° C
- Weight: 1.54lbs with no DRAM installed
- PC/104 expansion bus

  Female (non-stackthrough) 16-bit bus connectors, for expansion through PC/104 Version 2 double-stackthrough (DST) modules

  Four mounting holes
- 10-layer PCB using latest surface mount technology

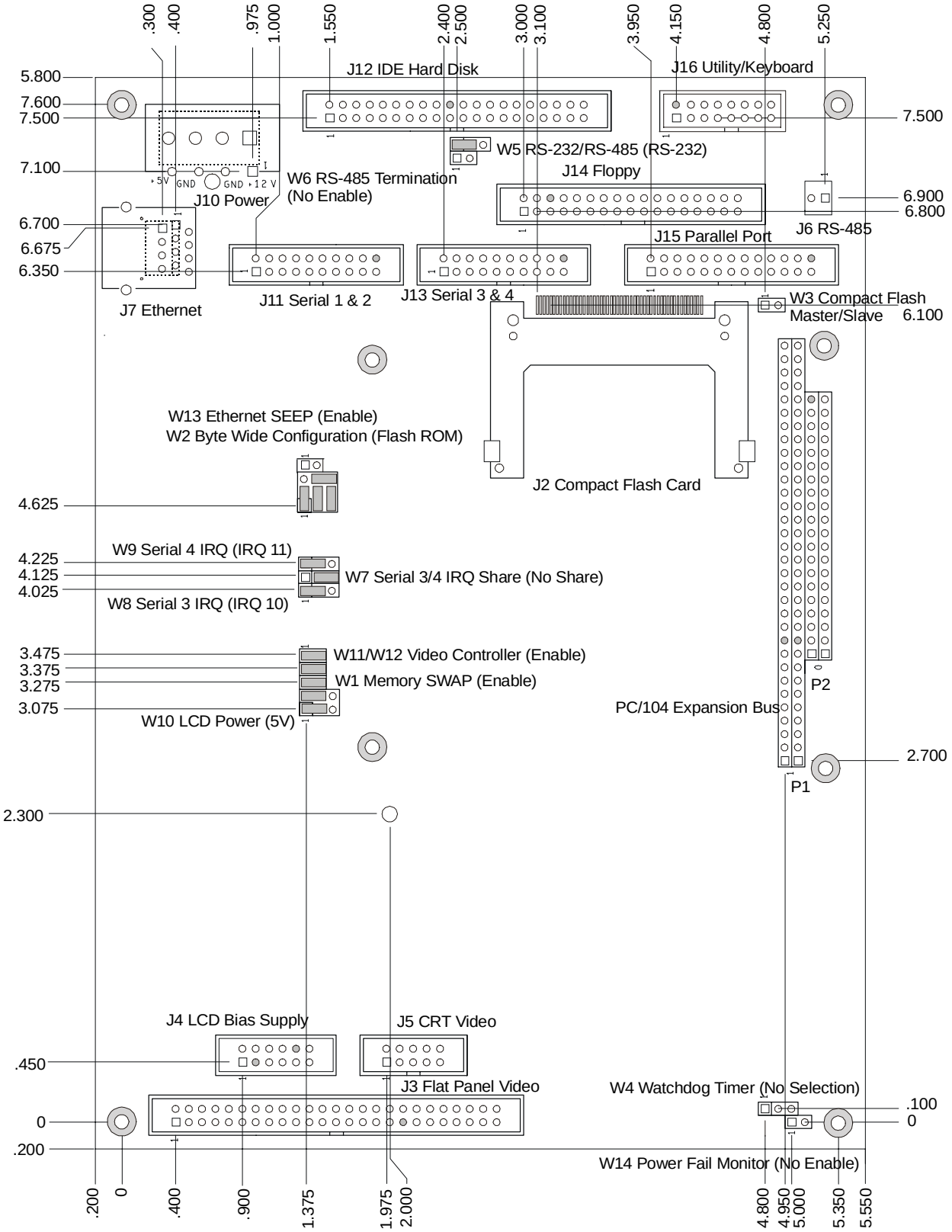


Figure 3–1. Mechanical Dimensions

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